

VHDL Libraries (1A)

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Conversion between bit and standard-logic types

<code>std_ulogic</code>	<code>to_std_logic</code>
<code>bit</code>	<code>to_bit</code>
<code>bit_vector</code>	<code>to_bv</code>
<code>sulv</code>	<code>to_sulv</code>
<code>slv</code>	<code>to_slv</code>

Conversion to unsigned and signed

unsigned

signed

to_unsigned

to_signed

Conversion to ufixed and sfixed

ufixed

to_ufixed

sfixed

to_sfixed

Conversion to float

float

to_float

Conversion to integer and real

integer

real

to_integer

to_real

The std_logic_1164 Package

The numeric_bit and numeric_std Packages

The numeric_std_unsigned

The Numeric Unsigned Packages

The Fixed-point Math Packages

The Floating-Point Math Packages

The Standard Packages

The Env Packages

References

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http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
- [3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
- [4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
- [5] D. Smith, HDL Chip Design
- [6] <http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html>
- [7] VHDL Tutorial - VHDL online www.vhdl-online.de/tutorial/
- [8] P. J. Ashenden, "The Designer's Guide to VHDL"