

Package (1C)

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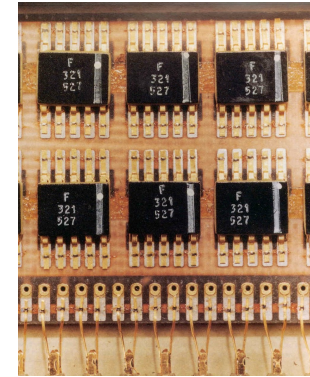
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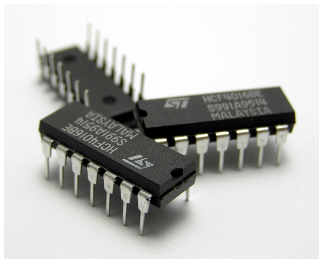
Package

the final stage of semiconductor device fabrication
the tiny block of semiconducting material is encased in a supporting case that prevents physical damage and corrosion.

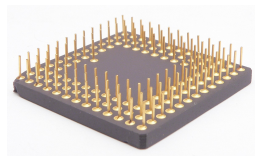
The case, known as a "package", supports the electrical contacts which connect the device to a circuit board.



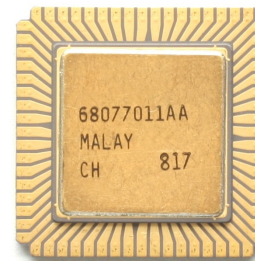
A TTL logic gate in a flat pack package



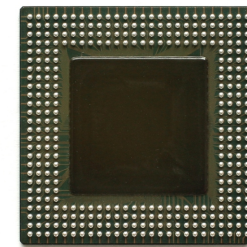
Three 14-pin (DIP14) plastic dual in-line packages containing IC chips.



The pin grid array at the bottom of a XC68020, a prototype of the Motorola 68020 microprocessor

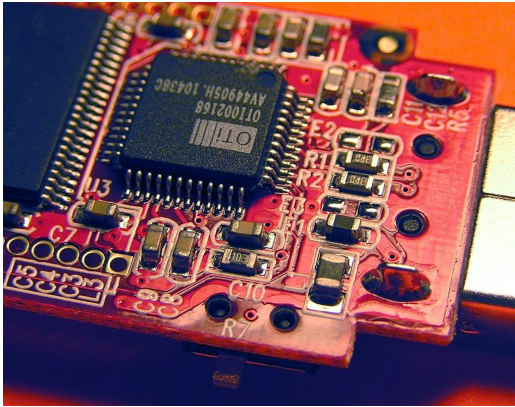


Ceramic Leadless package of Intel R80286-8 (bottom)[6]

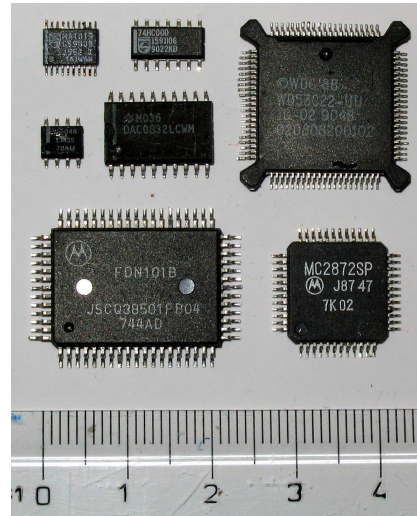


Bottom view of an Intel Embedded Pentium MMX, showing the blobs of solder

Surface Mount Technology



Surface-mount components on a USB flash drive's circuit board. The small rectangular chips with numbers are resistors, while the unmarked small rectangular chips are capacitors. The visible capacitors and resistors are predominantly a combination of 0805 and 0603 package sizes, while the smallest chip capacitors are 01005 size



Surface-mount technology (SMT) is a method for constructing electronic circuits in which the components are mounted directly onto the surface of printed circuit boards (PCBs). An electronic device so made is called a surface-mount device (SMD). In the industry it has largely replaced the through-hole technology construction method of fitting components with wire leads into holes in the circuit board. Both technologies can be used on the same board for components not suited to surface mounting such as transformers and heat-sinked power semiconductors.

Package Types (1)

Dual-in-line

flatpack was one of the earliest surface-mounted packages.

SOIC: (Small-Outline Integrated Circuit), dual-in-line, 8 or more pins, gull-wing lead form, pin spacing 1.27 mm

SOJ: Small-Outline Package, J-Leaded, the same as SOIC except J-leaded [2]

TSOP: Thin Small-Outline Package, thinner than SOIC with smaller pin spacing of 0.5 mm

SSOP: Shrink Small-Outline Package, pin spacing of 0.65 mm, sometimes 0.635 mm or in some cases 0.8 mm

TSSOP: Thin Shrink Small-Outline package.

QSOP: Quarter-Size Small-Outline package, with pin spacing of 0.635 mm

VSOP: Very Small Outline Package, even smaller than QSOP; 0.4, 0.5 mm or 0.65 mm pin spacing

DFN: Dual Flat No-lead, smaller footprint than leaded equivalent

Quad-in-line

PLCC: Plastic Leaded Chip Carrier, square, J-lead, pin spacing 1.27 mm

QFP: Quad Flat Package, various sizes, with pins on all four sides

LQFP: Low-profile Quad Flat Package, 1.4 mm high, varying sized and pins on all four sides

PQFP: Plastic Quad Flat-Pack, a square with pins on all four sides, 44 or more pins

CQFP: Ceramic Quad Flat-Pack, similar to PQFP

MQFP: Metric Quad Flat Pack, a QFP package with metric pin distribution

TQFP: Thin Quad Flat Pack, a thinner version of PQFP

QFN: Quad Flat No-lead, smaller footprint than leaded equivalent

LCC: Leadless Chip Carrier, contacts are recessed vertically to "wick-in" solder. Common in aviation electronics because of robustness to mechanical vibration.

MLP (MLF): Micro Leadframe Package (Micro Lead-Frame package) with a 0.5 mm contact pitch, no leads (same as QFN) [3]

PQFN: Power Quad Flat No-lead, with exposed die-pad[s] for heatsinking

Package Types (2)

Grid arrays

PGA: Pin grid array.

BGA: Ball Grid Array, with a square or rectangular array of solder balls on one surface, ball spacing typically 1.27 mm

LGA: An array of bare lands only. Similar to in appearance to QFN, but mating is by spring pins within a socket rather than solder.

FBGA: Fine pitch Ball Grid Array, with a square or rectangular array of solder balls on one surface

LFBGA: Low profile Fine pitch Ball Grid Array, with a square or rectangular array of solder balls on one surface, ball spacing typically 0.8 mm

TFBGA: Thin Fine pitch Ball Grid Array, with a square or rectangular array of solder balls on one surface, ball spacing typically 0.5 mm

CGA: Column Grid Array, circuit package in which the input and output points are high temperature solder cylinders or columns arranged in a grid pattern.

CCGA: Ceramic Column Grid Array, circuit package in which the input and output points are high temperature solder cylinders or columns arranged in a grid pattern. The body of the component is ceramic.

µBGA: micro-BGA, with ball spacing less than 1 mm

LLP: Lead Less Package, a package with metric pin distribution (0.5 mm pitch).

Non-packaged devices (although surface-mount, these devices require specific process for assembly):

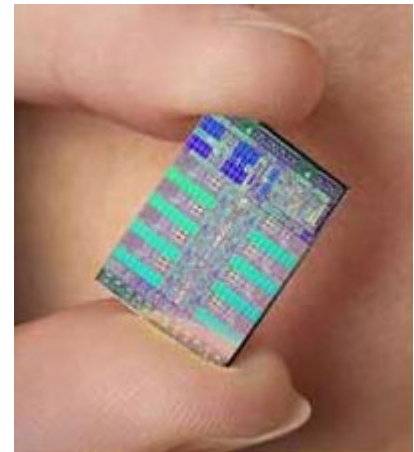
COB: Chip-On-Board; a bare silicon chip, that is usually an integrated circuit, is supplied without a package (usually a lead frame overmolded with epoxy) and is attached, often with epoxy, directly to a circuit board. The chip is then wire bonded and protected from mechanical damage and contamination by an epoxy "glob-top".

COF: Chip-On-Flex; a variation of COB, where a chip is mounted directly to a flex circuit.

COG: Chip-On-Glass; a variation of COB, where a chip, typically a Liquid crystal display (LCD) controller, is mounted directly on glass:.

Die

A die in the context of integrated circuits is a small block of semiconducting material, on which a given functional circuit is fabricated. Typically, integrated circuits are produced in large batches on a single wafer of electronic-grade silicon (EGS) or other semiconductor (such as GaAs) through processes such as photolithography. The wafer is cut (“diced”) into many pieces, each containing one copy of the circuit. Each of these pieces is called a die.



A cell processor die

Wafer Dicing

Wafer dicing is the process by which die are separated from a wafer of semiconductor following the processing of the wafer. The dicing process can be accomplished by scribing and breaking, by mechanical sawing (normally with a machine called a dicing saw) or by laser cutting. Following the dicing process the individual silicon chips are encapsulated into chip carriers which are then suitable for use in building electronic devices such as computers, etc.

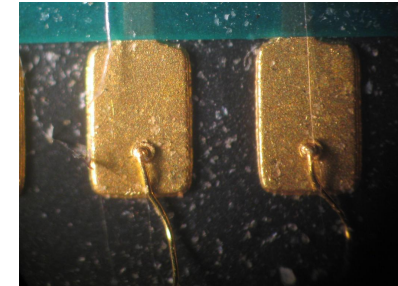
Wire Bonding

Wire bonding is the primary method of making interconnections between an integrated circuit (IC) and a printed circuit board (PCB) during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another. Wire bonding is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.

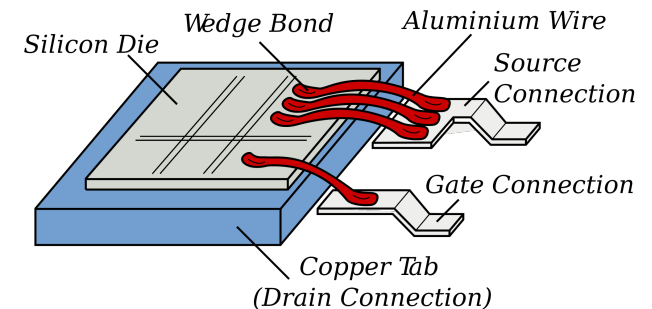
Bondwires usually consist of one of the following materials:

- Aluminum
- Copper
- Gold

Wire diameters start at 15 μm and can be up to several hundred micrometres for high-powered applications.



Gold wire ball-bonded to a gold contact pad



The interconnections in a power package are made using thick (250 to 400 μm), wedge-bonded, aluminium wires.

Multi Chip Module

A multi-chip module (MCM) is a specialized electronic package where multiple integrated circuits (ICs), semiconductor dies or other discrete components are packaged onto a unifying substrate, facilitating their use as a single component (as though a larger IC). The MCM itself will often be referred to as a "chip" in designs, thus illustrating its integrated nature.

System in Chip (SiP)

A system-in-a-package or system in package (SiP), also known as a Chip Stack MCM. A SiP is a number of integrated circuits enclosed in a single module (package). The SiP performs all or most of the functions of an electronic system, and are typically used inside a mobile phone, digital music player, etc. Dies containing integrated circuits, may be stacked vertically on a substrate. They are internally connected by fine wires that are bonded to the package. Alternatively, with a flip chip technology, solder bumps are used to join stacked chips together.

SiP dies are stacked vertically, unlike slightly less dense multi-chip modules, which place dies horizontally alongside one another. SiP connects the dies with standard off-chip wire bonds or solder bumps, unlike slightly denser three-dimensional integrated circuits which connect stacked silicon dies with conductors running through the die.

Flip Chip

- Integrated circuits are created on the wafer
- Pads are metalized on the surface of the chips
- Solder dots are deposited on each of the pads
- Chips are cut
- Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry
- Solder balls are then remelted (typically using hot air reflow)
- Mounted chip is “underfilled” using an electrically-insulating adhesive

Flip chip, also known as controlled collapse chip connection or its acronym, C4, is a method for interconnecting semiconductor devices, such as IC chips and microelectromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is flowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry.

Dielectric

References

- [1] <http://en.wikipedia.org/>
- [2] <http://planetmath.org/>
- [3] M.L. Boas, "Mathematical Methods in the Physical Sciences"