Logic Families

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Logic family

In computer engineering, a **logic family** may refer to one of two related concepts. A logic family of monolithic digital integrated circuit devices is a group of electronic logic gates constructed using one of several different designs, usually with compatible logic levels and power supply characteristics within a family. Many logic families were produced as individual components, each containing one or a few related basic logical functions, which could be used as "building-blocks" to create systems or as so-called "glue" to interconnect more complex integrated circuits. A "logic family" may also refer to a set of techniques used to implement logic within VLSI integrated circuits such as central processors, memories, or other complex functions. Some such logic families use static techniques to minimize design complexity. Other such logic families, such as domino logic, use clocked dynamic techniques to minimize size, power consumption, and delay.

Before the widespread use of integrated circuits, various solid-state and vacuum-tube logic systems were used but these were never as standardized and interoperable as the integrated-circuit devices.

Technologies

The list of packaged building-block logic families can be divided into categories, listed here in roughly chronological order of introduction, along with their usual abbreviations:

- Resistor–transistor logic (RTL)
  - Direct-coupled transistor logic (DCTL)
  - Resistor–capacitor–transistor logic (RCTL)
- Diode–transistor logic (DTL)
  - Complemented transistor diode logic (CTDL)
  - High-threshold logic (HTL)
- Emitter-coupled logic (ECL)
  - Positive emitter-coupled logic (PECL)
  - Low-voltage positive emitter-coupled logic (LVPECL)
- Gunning transceiver logic (GTL)
- Transistor–transistor logic (TTL)
- P-type metal–oxide–semiconductor logic (PMOS)
- N-type metal–oxide–semiconductor logic (NMOS)
  - Depletion-load NMOS logic
  - High-density nMOS (HMOS)
- Complementary metal–oxide–semiconductor logic (CMOS)
- Bipolar complementary metal–oxide–semiconductor logic (BiCMOS)
- Integrated injection logic (I^2L)

The families (RTL, DTL, and ECL) were derived from the logic circuits used in early computers, originally implemented using discrete components. One example is the Philips NORbits family of logic building blocks.

The PMOS and I^2L logic families were used for relatively short periods, mostly in special purpose custom large-scale integration circuits devices and are generally considered obsolete. For example, early digital clocks or electronic calculators may have used one or more PMOS devices to provide most of the logic for the finished product. The F14 CADC, Intel 4004, Intel 4040, and Intel 8008 microprocessors and their support chips were PMOS.

Of these families, only ECL, TTL, NMOS, CMOS, and BiCMOS are currently still in widespread use. ECL is used for very high-speed applications because of its price and power demands, while NMOS logic is mainly used in VLSI

circuits applications such as CPUs and memory chips which fall outside of the scope of this article. Present-day "building block" logic gate ICs are based on the ECL, TTL, CMOS, and BiCMOS families.

RTL

Main article: Resistor–transistor logic

The Atanasoff–Berry Computer used resistor-coupled vacuum tube logic circuits similar to RTL. Several early transistorized computers (e.g., IBM 1620, 1959) used RTL, where it was implemented using discrete components.

A family of simple resistor–transistor logic integrated circuits was developed at Fairchild Semiconductor for the Apollo Guidance Computer in 1962. Texas Instruments soon introduced its own family of RTL. A variant with integrated capacitors, RCTL, had increased speed, but lower immunity to noise than RTL. This was made by Texas Instruments as their "51XX" series.

DTL

Main article: Diode–transistor logic

Diode logic goes back as far as ENIAC and was used in many early vacuum tube computers. Several early transistorized computers (e.g., IBM 1401) used DTL, where it was implemented using discrete components.

The first diode–transistor logic family of integrated circuits was introduced by Signetics in 1962. DTL was also made by Fairchild and Westinghouse. A family of diode logic and diode-transistor logic integrated circuits was developed by Texas Instruments for the D-37C Minuteman II Guidance Computer in 1962, but these devices were not available to the public.

A variant of DTL called "high-threshold logic" incorporated Zener diodes to create a large offset between logic 1 and logic 0 voltage levels. These devices usually ran off a 15 volt power supply and were found in industrial control, where the high differential was intended to minimize the effect of noise.[1]

ECL

Main article: Emitter-coupled logic

The ECL family, ECL is also known as current-mode logic (CML), was invented by IBM as current steering logic for use in the transistorized IBM 7030 Stretch computer, where it was implemented using discrete components.

The first ECL logic family to be available in integrated circuits was introduced by Motorola as *MECL* in 1962.[2]

TTL

Main article: Transistor–transistor logic

The first transistor-transistor logic family of integrated circuits was introduced by Sylvania as *Sylvania Universal High–Level Logic* (SUHL) in 1963. Texas Instruments introduced 5400 Series TTL family in 1964. Transistor–transistor logic uses bipolar transistors to form its integrated circuits.[3] TTL has changed significantly over the years, with newer versions replacing the older types.

Since the transistors of a standard TTL gate are saturated switches, minority carrier storage time in each junction limits the switching speed of the device. Variations on the basic TTL design are intended to reduce these effects and improve speed, power consumption, or both.

The German physicist Walter H. Schottky formulated a theory predicting the **Schottky effect**, which led to the Schottky diode and later Schottky transistors. Schottky transistors have a much higher switching speed than conventional transistors because the Schottky junction does not promote charge storage, leading to faster switching gates. Gates built with Schottky transistors use more power than normal TTL and switch faster. With **Low-power**

Schottky (LS), internal resistance values were increased to reduce power consumption and increase switching speed over the original version. The introduction of **Advanced Low-power Schottky** (ALS) further increased speed and reduced power consumption. A faster logic family called **Fast** (Schottky) (F) was also introduced that was faster than normal Schottky TTL.

IIL

Main article: integrated injection logic

The integrated injection logic (IIL or I^2L) uses bipolar transistors in a kind of current-steering arrangement to form its integrated circuits. IIL is slightly easier to construct on an integrated circuit, and so was popular for early VLSI circuits.

CMOS

Main article: CMOS

CMOS logic gates use complementary arrangements of N-channel and P-channel Field effect transistor. Since the initial devices used oxide-isolated metal gates, they were called **CMOS** (complementary metal–oxide–semiconductor logic). In contrast to TTL, CMOS uses almost no power in the static state (that is, when inputs are not changing). A CMOS gate draws no current other than leakage when in a steady 1 or 0 state. When the gate switches states, current is drawn from the power supply to charge the capacitance at the output of the gate. This means that the current draw of CMOS devices increases with switching rate (controlled by clock speed, typically).

The first CMOS family of logic integrated circuits was introduced by RCA as *CD4000 COS/MOS*, the 4000 series, in 1968. Initially CMOS logic was slower than LS-TTL. However, because the logic thresholds of CMOS were proportional to the power supply voltage, CMOS devices were well-adapted to battery-operated systems with simple power supplies. CMOS gates can also tolerate much wider voltage ranges than TTL gates because the logic thresholds are (approximately) proportional to power supply voltage, and not the fixed levels required by bipolar circuits.

The required silicon area for implementing such digital CMOS functions has rapidly shrunk. VLSI technology incorporating millions of basic logic operations onto one chip, almost exclusively uses CMOS. The extremely small capacitance of the on-chip wiring, caused an increase in performance by several orders of magnitude. On-chip clock rates as high as 4 GHz have become common, approximately 1000 times faster than the technology by 1970.

Lowering the power supply voltage

CMOS chips often work with a broader range of power supply voltages than other logic families. Early TTL ICs required a power supply voltage of 5V, but early CMOS could use 3 to 15V.[4] Lowering the supply voltage reduces the charge stored on any capacitances and consequently reduces the energy required for a logic transition. Reduced energy implies less heat dissipation. The energy stored in a capacitance C and changing V volts is $\frac{1}{2} CV^2$. By lowering the power supply from 5V to 3.3V, switching power was reduced by almost 60 percent (power dissipation is proportional to the square of the supply voltage). Newer CPUs have lowered their power supply voltages further.

HC logic

Because of the incompatibility of the CD4000 series of chips with the previous TTL family, a new standard emerged which combined the best of the TTL family with the advantages of the CD4000 family. It was known as the 74HC (High-performance silicon gate) family of devices and used the pinout of the 74LS family with an improved version of CMOS technology inside the chip. It could be used both with logic devices which used 3.3V power supplies (and thus 3.3V logic levels), and with devices that used 5V power supplies and TTL logic levels.

The CMOS–TTL logic level problem

Interconnecting any two logic families often required special techniques such as additional pull-up resistors, or purpose-built interface circuits, since the logic families may use different voltage levels to represent 1 and 0 states, and may have other interface requirements only met within the logic family.

TTL logic levels are different from those of CMOS – generally a TTL output does not rise high enough to be reliably recognized as a logic 1 by a CMOS input. This problem was solved by the invention of the 74HCT family of devices that uses CMOS technology but TTL input logic levels. These devices only work with a 5V power supply. They form a replacement for TTL, although HCT is slower than original TTL (HC logic has about the same speed as original TTL).

Other CMOS families

Other CMOS circuit families within integrated circuits include cascode voltage switch logic (CVSL) and pass transistor logic (PTL) of various sorts. These are generally used "on-chip" and are not delivered as building-block medium-scale or small-scale integrated circuits.

BiCMOS

Main article: BiCMOS

One major improvement was to combine CMOS inputs and TTL drivers to form of a new type of logic devices called BiCMOS logic, of which the LVT and ALVT logic families are the most important. The BiCMOS family has many members, including ABT logic, ALB logic, ALVT logic, BCT logic and LVT logic.

Improved versions

With HC and HCT logic and LS-TTL logic competing in the market it became clear that further improvements were needed to create the *ideal* logic device that combined high speed, with low power dissipation and compatibility with older logic families. A whole range of newer families has emerged that use CMOS technology. A short list of the most important family designators of these newer devices includes:

- LV logic (lower supply voltage)
- LVT logic (lower supply voltage while retaining TTL logic levels)
- ALVT logic (an 'advanced' version of LVT logic)

There are many others including AC/ACT logic, AHC/AHCT logic, ALVC logic, AUC logic, AVC logic, CBT logic, CBTLV logic, FCT logic and LVC logic (LVCMOS).

Monolithic integrated circuit logic families compared

The following logic families would either have been used to build up systems from functional blocks such as flip-flops, counters, and gates, or else would be used as "glue" logic to interconnect very-large scale integration devices such as memory and processors. Not shown are some early obscure logic families from the early 1960s such as DCTL (direct-coupled transistor logic), which did not become widely available.

Propagation delay is the time taken for a two-input NAND gate to produce a result after a change of state at its inputs. *Toggle speed* represents the fastest speed at which a J-K flip flop could operate. *Power per gate* is for an individual 2-input NAND gate; usually there would be more than one gate per IC package. Values are very typical and would vary slightly depending on application conditions, manufacturer, temperature, and particular type of logic circuit. *Introduction year* is when at least some of the devices of the family were available in volume for civilian uses. Some military applications pre-dated civilian use.[5][6]

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic	500	4	10	3.3	1963	the first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.
DTL	Diode–transistor logic	25		10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)		1.65 - 3.6	2004	First GHz 7400 series logic
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8		31	-5.2	1962	first integrated logic circuit commercially produced
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	

On-chip design styles

Several techniques and design styles are primarily used in designing large single-chip application-specific integrated circuits (ASIC) and CPUs, rather than generic logic families intended for use in multi-chip applications.

These design styles can typically be divided into two main categories, static techniques and clocked dynamic techniques. (See static versus dynamic logic for some discussion on the advantages and disadvantages of each category).

Static logic

- Pulsed Static CMOS
- Differential Cascode Voltage Switch (DCVS)
- Cascode Non-Threshold Logic (CNTL)
- Pass Gate/Transmission Gate Logic: pass transistor logic (PTL)
- Complementary Pass Gate Logic (CPL)
- Push-Pull Logic
- Output Prediction Logic (OPL)
- cascode voltage switch logic (CVSL)

Dynamic logic

- four-phase logic
- domino logic
- Footless Domino
- NORA/Zipper Logic
- Multiple-Output Domino
- Compound Domino
- Dual-Rail Domino
- Self-Resetting Domino
- Sample-Set Differential Logic
- Limited Switch Dynamic Logic

References

[1] Jacob Millman, *Microelectronics Digital and Analog Circuits and Systems*, McGraw-Hill Book Company, New York, 1979, ISBN 0-07-042327-X

[2] William R. Blood Jr. (1972). *MECL System Design Handbook* 2nd ed. n.p.: Motorola Semiconductor Products Inc. vi.

[3] Don Lancaster, *TTL Cookbook*, Howard W. Sams and Co., Indianapolis, 1975, ISBN 0-672-21035-5

[4] RCA COSMOS

[5] The Engineering Staff, *The TTL Data Book for Design Engineers*, 1st Ed., Texas Instruments, Dallas Texas, 1973, no ISBN, pages 59 , 87

[6] Paul Horowitz and Winfield Hill, *The Art of Electronics 2nd Ed.* Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7 table 9.1 page 570

Further reading

- H. P. Westman (ed), *Reference Data for Radio Engineers 5th Edition*, Howard W. Sams & Co., Indianapolis, 1968, no ISBN, Library of Congress Card 43-14665

External links

- What Computers are Made From (http://www.quadibloc.com/comp/cp01.htm)

Resistor–transistor logic

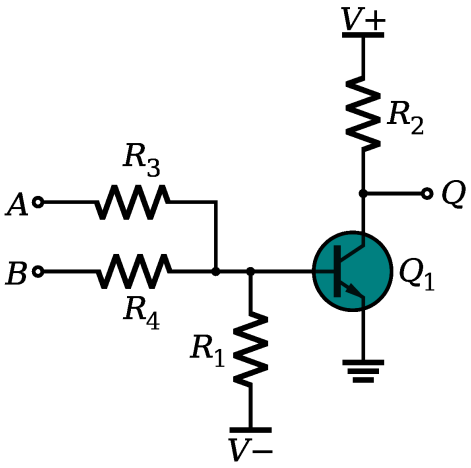
Resistor–transistor logic (**RTL**) is a class of digital circuits built using resistors as the input network and bipolar junction transistors (BJTs) as switching devices. RTL is the earliest class of transistorized digital logic circuit used; other classes include diode–transistor logic (DTL) and transistor–transistor logic (TTL). The concept had been used in early computers with electron tubes, and in RTL circuits constructed with discrete components, but in 1961 it became the first digital logic family to be produced as a monolithic integrated circuit. Such were used in the US space program in 1962.

Implementation

RTL inverter

A bipolar transistor switch is the simplest RTL gate (inverter or NOT gate) implementing logical negation.[1] It consists of a common-emitter stage with a base resistor connected between the base and the input voltage source. The role of the base resistor is to expand the negligible transistor input voltage range (about 0.7 V) to the logical "1" level (about 3.5 V) by converting the input voltage into current. Its resistance is settled by a compromise: it is chosen low enough to saturate the transistor and high enough to obtain high input resistance. The role of the collector resistor is to convert the collector current into voltage; its resistance is chosen high enough to saturate the transistor and low enough to obtain low output resistance (high fan-out).

One-transistor RTL NOR gate

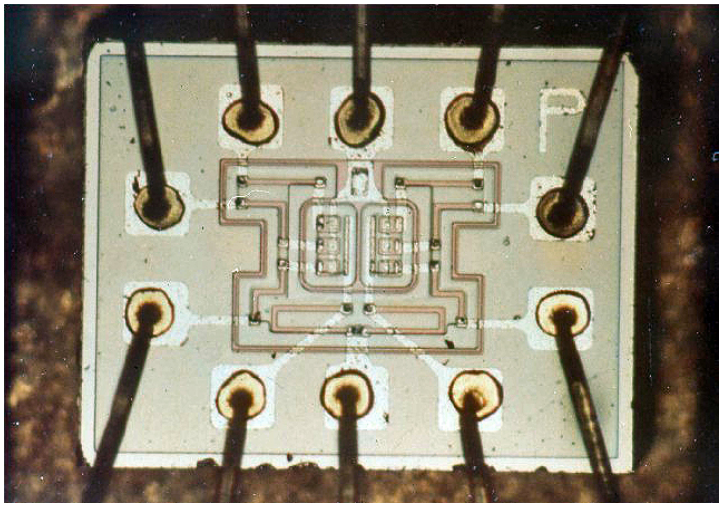


Schematic of a one-transistor RTL NOR gate.

By connecting additional base resistors (R_3 and R_4) to the inverter it is expanded to the simplest RTL NOR gate (see the figure on the right). It is an interesting fact that the basic input logical operation OR is performed by applying consecutively the two arithmetic operations addition and comparison (the input resistor network acts as a parallel *voltage summer* with equally weighted inputs and the next common-emitter transistor stage - as a *voltage comparator* with a threshold about 0.7 V). The equivalent resistance of all the resistors connected to logical "1" and the equivalent resistance of all the resistors connected to logical "0" form the two legs of a composed voltage divider driving the transistor. The base resistances and the number of the inputs are chosen (limited) so that only one logical "1" is sufficient to create base-emitter voltage exceeding the threshold and, as a result, saturating the transistor. If all the input voltages are low (logical "0"), the transistor is cut-off. The pull-down resistor R_1 provides reliable cut-off of the transistor (it is not absolutely necessary in the case of a silicon transistor). The output is inverted since the voltage drop across the collector-emitter junction of the transistor Q_1 is taken as a grounded output instead the voltage drop across the floating collector resistor R_2. Thus, the analog resistive network and the analog transistor stage perform the logic function NOR.

Multi-transistor RTL NOR gate

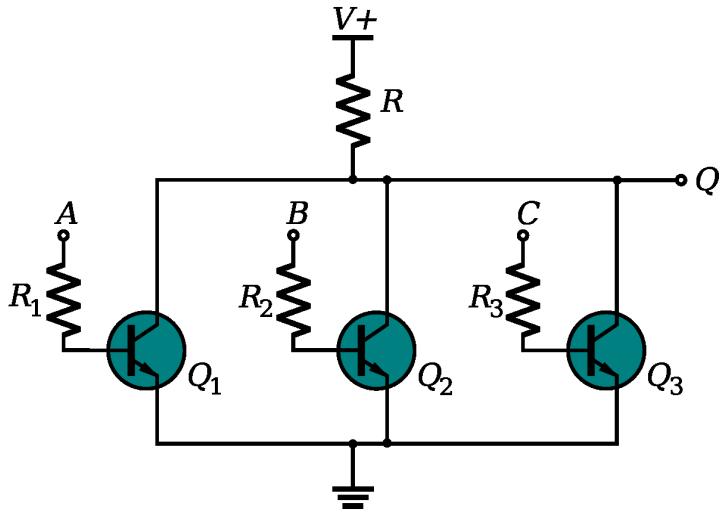
The limitations of the one-transistor RTL NOR gate are overcome by the multi-transistor RTL implementation. It consists of a set of parallel-connected transistor switches driven by the logic inputs (see the figure on the right). In this configuration, the inputs are completely separated and the number of inputs is limited only by the small reverse saturation current of the cut-off transistors at output logical "1". The same idea is used later for building DCTL, ECL, some TTL (7450, 7460), NMOS and CMOS gates.



photograph of the dual NOR gate chip used to build the Apollo Guidance Computer

Advantages

The primary advantage of RTL technology was that it involved a minimum number of transistors, which was an important consideration before integrated circuit technology (that is, in circuits using discrete components), as transistors were the most expensive component to produce. Early IC logic production (such as Fairchild's in 1961) used the same approach briefly, but quickly transitioned to higher-performance circuits such as diode–transistor logic and then transistor–transistor logic (starting 1963 at Sylvania), since diodes and transistors were no more expensive than resistors in the IC.



Schematic of a multi-transistor RTL NOR gate used to build the Apollo Guidance Computer[2]

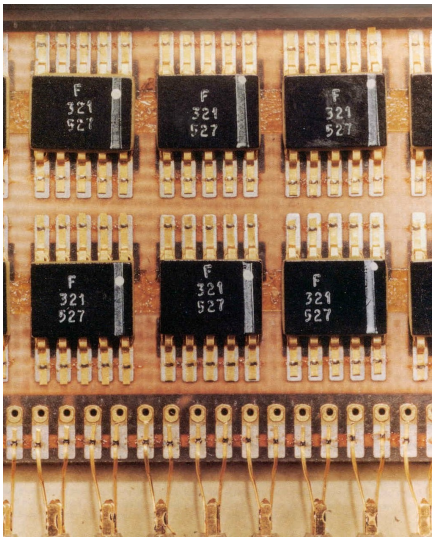
Limitations

The obvious disadvantage of RTL is its high power dissipation when the transistor is switched on (the power is dissipated mainly by the base resistors connected to logical "1" and by the collector resistor). This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits with "totem-pole" output stage minimize both of these

requirements. Another limitation of RTL was its limited fan-in: 3 inputs being the limit for many circuit designs, before it completely lost usable noise immunity.Wikipedia:Citation needed It has a low noise margin.

Lancaster says that integrated circuit RTL NOR gates (which have one transistor per input) may be constructed with "any reasonable number" of logic inputs, and gives an example of an 8-input NOR gate.

A standard integrated circuit RTL NOR gate can drive up to 3 other similar gates. Alternatively, it has enough output to drive up to 2 standard integrated circuit RTL "buffers", each of which can drive up to 25 other standard RTL NOR gates.



Flatpack RTL NOR gate integrated circuits in the Apollo guidance computer

Speeding up RTL

Various companies applied the following speed-up methods to discrete RTL.

Transistor switching speed has increased steadily from the first transistorized computers through the present. The *GE Transistor Manual* (7th ed., p. 181, or 3rd ed., p. 97 or intermediate editions) recommends gaining speed by using higher-frequency transistors, or capacitors, or a diode from base to collector (parallel negative feedback) to prevent saturation.

Placing a capacitor in parallel with each input resistor decreases the time needed for a driving stage to forward-bias a driven stage's base-emitter junction. Engineers and technicians use “RCTL” (resistor capacitor transistor logic) to designate gates equipped with “speed-up capacitors.” The Lincoln Laboratory TX-0 computer's circuits included some RCTL. However, methods involving capacitors were unsuitable for integrated circuits.Wikipedia:Citation needed

Using a high collector supply voltage and diode clamping decreased collector-base and wiring capacitance charging time. This arrangement required diode clamping the collector to the design logic level. This method was also applied to discrete DTL (diode–transistor logic).

Another method that was familiar in discrete-device logic circuits used a diode and a resistor, a germanium and a silicon diode, or three diodes in a negative feedback arrangement. These diode networks known as various Baker clamps reduced the voltage applied to the base as the collector approached saturation. Because the transistor went less deeply into saturation, the transistor accumulated fewer stored charge carriers. Therefore, less time was required to clear stored charge during transistor turn off. A low-voltage diode arranged to prevent saturation of the transistor was applied to integrated logic families by using Schottky diodes, as in Schottky TTL.

References

[1] Resistor-Transistor Logic (http://www.play-hookey.com/digital_electronics/rtl_gates.html) explains the basic RTL gates and gives some useful calculations

[2] Apollo Guidance Computer schematics, Dwg. No. 2005011 (http://klabs.org/history/ech/agc_schematics/logic/5011-1.jpg).

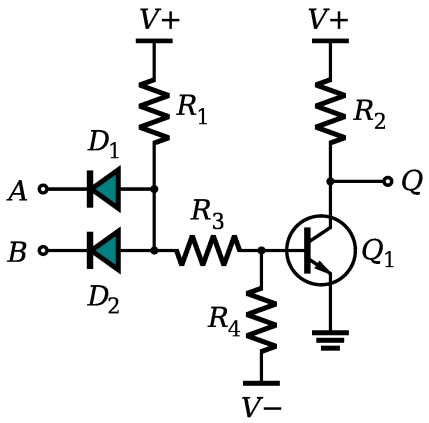
Diode–transistor logic

"DTL" redirects here. For other uses, see DTL (disambiguation).

Diode–transistor logic (**DTL**) is a class of digital circuits that is the direct ancestor of transistor–transistor logic. It is called so because the logic gating function (e.g., AND) is performed by a diode network and the amplifying function is performed by a transistor (in contrast with RTL and TTL).

Implementations

The DTL circuit shown in the picture consists of three stages: an input diode logic stage (D1, D2 and R1), an intermediate level shifting stage (R3, R4 and V−) and an output common-emitter switching-transistor stage (Q1 and R2). The two resistors R3 and R4 form a resistive summing circuit with weighted inputs that adds the negative bias voltage V− to the positive diode logic output voltage. As a result, the unipolar (positive) diode output voltage (about V+ for *logical one* and 1.0 V for *logical zero*) is converted into a bipolar voltage (a few volts above and below ground) to drive the output transistor.



Schematic of basic two-input DTL NAND gate. R3, R4 and V− shift the positive output voltage of the input DL stage below the ground (to cut off the transistor at low input voltage).

The IBM 1401 (announced in 1959[1]) used DTL circuits similar to the simplified circuit.[2] IBM called the logic "complemented transistor diode logic" (CTDL). CTDL avoided the level shifting stage (R3, R4, and V−) by alternating NPN- and PNP-based gates operating on different power supply voltages. The 1401 used germanium transistors and diodes in its basic gates. The 1401 also added an inductor in series with R2.[] The physical packaging used the IBM Standard Modular System.

In an integrated circuit version of the DTL gate, R3 is replaced by two level-shifting diodes connected in series. Also the bottom of R4 is connected to ground to provide bias current for the diodes and a discharge path for the transistor base. The resulting integrated circuit runs off a single power supply voltage.[3][4]

Speed acceleration

The DTL propagation delay is relatively large. When the transistor goes into saturation from all inputs being high, charge is stored in the base region. When it comes out of saturation (one input goes low) this charge has to be removed and will dominate the propagation time. A Baker clamp can be used to keep the transistor from saturating.

Another way to speed up DTL is to add a small capacitor across R3. The capacitor helps to turn off the transistor by removing the stored base charge; the capacitor also helps to turn on the transistor by increasing the initial base drive.[5]

Interfacing considerations

A major advantage over the earlier resistor–transistor logic is the increased fan-in. Alternatively, to increase fan-out of the gate, an additional transistor and diode may be used.

References

[1] computermuseum.li (http://www.computermuseum.li/Testpage/IBM-1401.htm)

[2] The IBM 1401 may have also used a current mode logic.

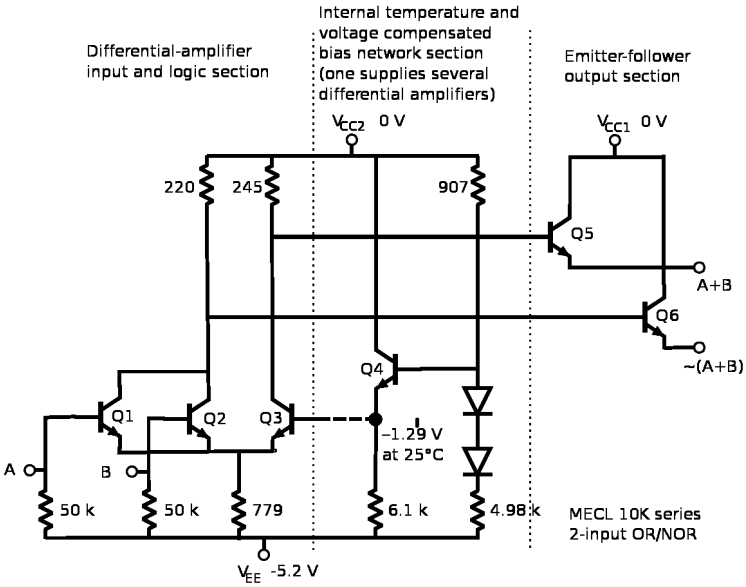
[3] , page 188 states resistor is replaced with one or more diodes; figure 10-43 shows 2 diodes; cites to Schulz 1962.

[4] ASIC world: "Diode Transistor Logic" (http://www.asic-world.com/digital/logic2.html)

[5] . Page 32 states: "As the input signal changes, the charge on the capacitor is forced into the base of the transistor. This charge can effectively cancel the transistor stored charge, resulting in a reduction of storage time. This method is very effective if the output impedance of the preceding stage is low so that the peak reverse current into the transistor is high."

Emitter-coupled logic

In electronics, **emitter-coupled logic (ECL)** is a high-speed integrated circuit bipolar transistor logic family. ECL uses an overdriven BJT differential amplifier with single-ended input and limited emitter current to avoid the saturated (fully on) region of operation and its slow turn-off behavior. As the current is steered between two legs of an emitter-coupled pair, ECL is sometimes called *current-steering logic* (CSL), *current-mode logic* (CML) or *current-switch emitter-follower* (CSEF) logic.



Motorola ECL 10,000 basic gate circuit diagram[1]

In ECL, the transistors are never in saturation, the input/output voltages have a small swing (0.8 V), the input impedance is high and the output resistance is low; as a result, the transistors change states quickly, gate delays are low, and the fanout capability is high. In addition, the essentially-constant current draw of the differential amplifiers minimises delays and glitches due to supply-line inductance and capacitance, and the complementary outputs decrease the propagation time of the whole circuit by saving additional inverters.

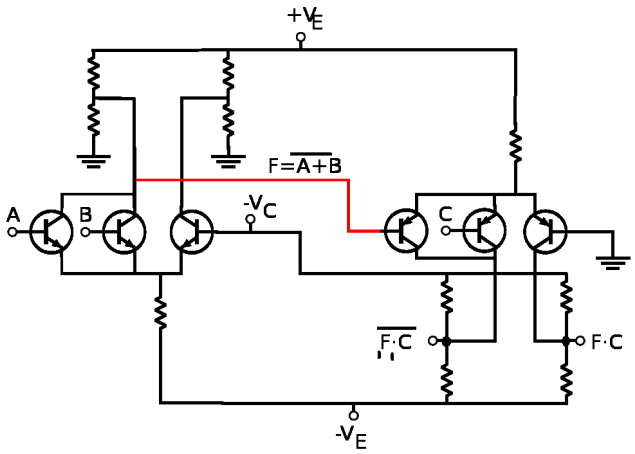
ECL's major disadvantage is that each gate continuously draws current, which means it requires (and dissipates) significantly more power than those of other logic families, especially when quiescent.

The equivalent of emitter-coupled logic made out of FETs is called source-coupled logic (SCFL).

A variation of ECL in which all signal paths and gate inputs are differential is known as differential current switch (DCS) logic.

History

ECL was invented in August 1956 at IBM by Hannon S. Yourke.[2][3] Originally called *current-steering logic*, it was used in the Stretch, IBM 7090, and IBM 7094 computers. The logic was also called a current mode circuit.[4]



Yourke's current switch, c. 1955.

Yourke's current switch, also known as ECL, was a differential amplifier, and the input logic levels were different from the output logic levels. "In current mode operation, however, the output signal consists of voltage levels which vary about a reference level different from the input reference level." In Yourke's design, the two logic reference levels differed by 3 volts. Consequently, two complementary versions were used: an NPN version and a PNP version. The NPN output could drive PNP inputs, and vice-versa. "The disadvantages are that more different power supply voltages are needed, and both pnp and npn transistors are required."

Instead of alternating NPN and PNP stages, another coupling method employed zener diodes and resistors to shift the output logic levels to be the same as the input logic levels.

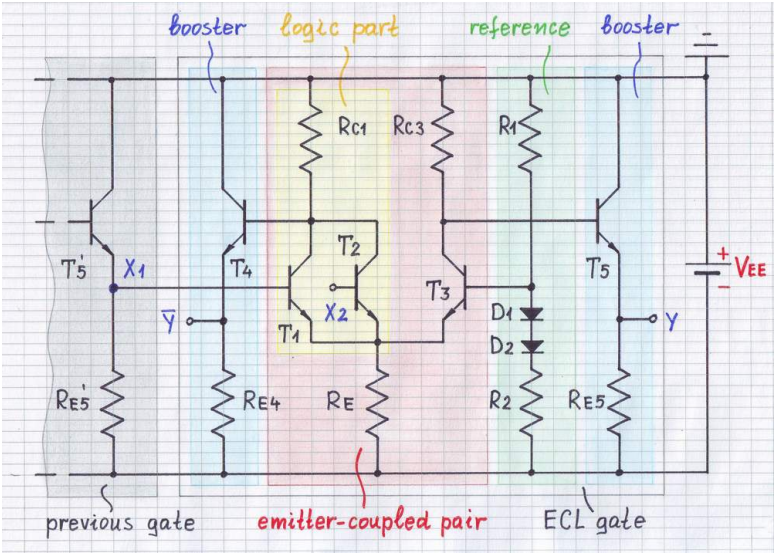
ECL circuits in the mid-1960s through the 1990s consisted of a differential amplifier input stage to perform logic, followed by an emitter follower to drive outputs and shift the output voltages so they will be compatible with the inputs.Wikipedia:Disputed statement

Motorola introduced their first digital monolithic integrated circuit line, MECL I, in 1962. Motorola developed several improved series, with MECL II in 1966, MECL III in 1968 with 1 nanosecond gate propagation time and 300 MHz flip-flop toggle rates, and the 10,000 series (with lower power consumption and controlled edge speeds) in 1971.[5]

The high power consumption associated with ECL has meant that it has been used mainly when high speed is a vital requirement. Older high-end mainframe computers, such as the Enterprise System/9000 members of IBM's ESA/390 computer family, used ECL as did the Cray-1; and first generation Amdahl mainframes. Current IBM mainframes use CMOS.

Implementation

ECL is based on an emitter-coupled (long-tailed) pair, shaded red in the figure on the right. The left half of the pair (shaded yellow) consists of two parallel-connected input transistors T1 and T2 (an exemplary two-input gate is considered) implementing NOR logic. The base voltage of the right transistor T3 is held fixed by a reference voltage source, shaded light green: the voltage divider with a diode thermal compensation (R1, R2, D1 and D2) and sometimes a buffering emitter follower (not shown on the picture); thus the emitter voltages are kept relatively steady. As a result, the common emitter resistor R_E acts nearly as a current source. The output voltages at the collector load resistors R_{C1} and R_{C3} are shifted and buffered to the inverting and non-inverting outputs by the emitter followers T4 and T5 (shaded blue). The output emitter resistors R_{E4} and R_{E5} do not exist in all versions of ECL. In some cases 50 Ω line termination resistors connected between the bases of the input transistors and −2 V act as emitter resistors.[6]



The picture represents a typical ECL circuit diagram based on Motorola's MECL. In this schematic, transistor T5′ represents the output transistor of a previous ECL gate that provides a logic signal to input transistor T1 of an OR/NOR gate whose other input is at T2 and has outputs Y and Y. Additional pictures illustrate the circuit operation by visualizing the voltage relief and current topology at low input voltage (logical "0"), during the transition and at high input voltage (logical "1").

Operation

The ECL circuit operation is considered below with assumption that the input voltage is applied to T1 base, while T2 input is unused or a logical "0" is applied.

During the transition, the core of the circuit – the emitter-coupled pair (T1 and T3) – acts as a differential amplifier with single-ended input. The "long-tail" current source (R_E) sets the total current flowing through the two legs of the pair. The input voltage controls the current flowing through the transistors by sharing it between the two legs, steering it all to one side when not near the switching point. The gain is higher than at the end states (see below) and the circuit switches quickly.

At low input voltage (logical "0") or at high input voltage (logical "1") the differential amplifier is overdriven. The one transistor (T1 or T3) is cut-off and the other (T3 or T1) is in active linear region acting as a common-emitter stage with emitter degeneration that takes all the current, starving the other cut-off transistor.

The active transistor is loaded with the relatively high emitter resistance R_E that introduces a significant negative feedback (emitter degeneration). To prevent saturation of the active transistor so that the diffusion time that slows the recovery from saturation will not be involved in the logic delay, the emitter and collector resistances are chosen such that at maximum input voltage some voltage is left across the transistor. The residual gain is low ($K = R_C/R_E < 1$). The circuit is insensitive to the input voltage variations and the transistor stays firmly in active linear region. The input resistance is high because of the series negative feedback.

The cut-off transistor breaks the connection between its input and output. As a result, its input voltage does not affect the output voltage. The input resistance is high again since the base-emitter junction is cut-off.

Characteristics

Other noteworthy characteristics of the ECL family include the fact that the large current requirement is approximately constant, and does not depend significantly on the state of the circuit. This means that ECL circuits generate relatively little power noise, unlike many other logic types which typically draw far more current when switching than quiescent, for which power noise can become problematic. In cryptographic applications, ECL circuits are also less susceptible to side channel attacks such as differential power analysis.

The propagation time for this arrangement can be less than a nanosecond, making it for many years the fastest logic family.

Power supplies and logic levels

The ECL circuits usually operate with negative power supplies (positive end of the supply is connected to ground) in contrast to other logic families in which negative end of the supply is grounded. This is done mainly to minimize the influence of the power supply variations on the logic levels as ECL is more sensitive to noise on the V_{CC} and relatively immune to noise on V_{EE}.[7] Because ground should be the most stable voltage in a system, ECL is specified with a positive ground. In this connection, when the supply voltage varies, the voltage drops across the collector resistors change slightly (in the case of emitter constant current source, they do not change at all). As the collector resistors are firmly "tied up" to ground, the output voltages "move" slightly (or not at all). If the negative end of the power supply was grounded, the collector resistors would be attached to the positive rail. As the constant voltage drops across the collector resistors change slightly (or not at all), the output voltages follow the supply voltage variations and the two circuit parts act as constant current level shifters. In this case, the voltage divider R1-R2 compensates the voltage variations to some extent. The positive power supply has another disadvantage - the output voltages will vary slightly (±0.4 V) against the background of high constant voltage (+3.9 V). Another reason for using a negative power supply is protection of the output transistors from an accidental short circuit developing between output and ground[8] (but the outputs are not protected from a short circuit with the negative rail).

The value of the supply voltage is chosen so that a sufficient current to flow through the compensating diodes D1 and D2 and the voltage drop across the common emitter resistor R_E to be adequate.

ECL circuits available on the open market usually operated with logic levels incompatible with other families. This meant that interoperation between ECL and other logic families, such as the popular TTL family, required additional interface circuits. The fact that the high and low logic levels are relatively close meant that ECL suffers from small noise margins, which can be troublesome.

At least one manufacturer, IBM, made ECL circuits for use in the manufacturer's own products. The power supplies were substantially different from those used in the open market.

Positive emitter-coupled logic (PECL) is a further development of ECL using a positive 5V supply instead of a negative 5.2V supply. Low-voltage positive emitter-coupled logic (LVPECL) is a power optimized version of PECL, using a positive 3.3V instead of 5V supply. PECL and LVPECL are differential signaling systems, and are mainly used in high speed and clock distribution circuits.

Logic levels:[9]

Type	V_{ee}	V_{low}	V_{high}	V_{cc}	V_{cm}
PECL	GND	3.4 V	4.2 V	5.0 V	
LVPECL	GND	1.6 V	2.4 V	3.3 V	2.0 V

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[7] Electronic Materials Handbook: Packaging (page 163) (http://books.google.bg/books?id=c2YxCCaM9RIC&pg=PA163&lpg=PA163&dq=5.2+V+power+supply+voltage+why&source=bl&ots=0eJCoqu1gf&sig=Wb9Cfd8EGOfqIOl_oNjdhVKUYdQ&hl=en&ei=ek_ESub7LYuz4QbApdw_&sa=X&oi=book_result&ct=result&resnum=6#v=onepage&q=5.2 V power supply voltage why&f=false) by Merrill L. Minges, ASM International. Handbook Committee

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External links

- Motorola MECL logic family datasheets, 1963 (http://www.wps.com/archives/solid-state-datasheets/Motorola/MECL/index.html)

Gunning transceiver logic

Gunning transceiver logic or **GTL** is a type of logic signaling used to drive electronic backplane buses. It has a voltage swing between 0.4 volts and 1.2 volts—much lower than that used in TTL and CMOS logic—and symmetrical parallel resistive termination. The maximum signaling frequency is specified to be 100 MHz, although some applications use higher frequencies. GTL is defined by JEDEC standard JESD 8-3 (1993) and was invented by William Gunning while working for Xerox at the Palo Alto Research Center.

All Intel front-side buses use GTL. As of 2008, GTL in these FSBs has a maximum frequency of 1.6 GHz. The front-side bus of the Intel Pentium Pro, Pentium II and Pentium III microprocessors uses GTL+ (or GTLP) developed by Fairchild Semiconductor, an upgraded version of GTL which has defined slew rates and higher voltage levels. AGTL+ stands for either assisted Gunning transceiver logic or advanced Gunning transceiver logic. These are GTL signaling derivatives used by Intel microprocessors.

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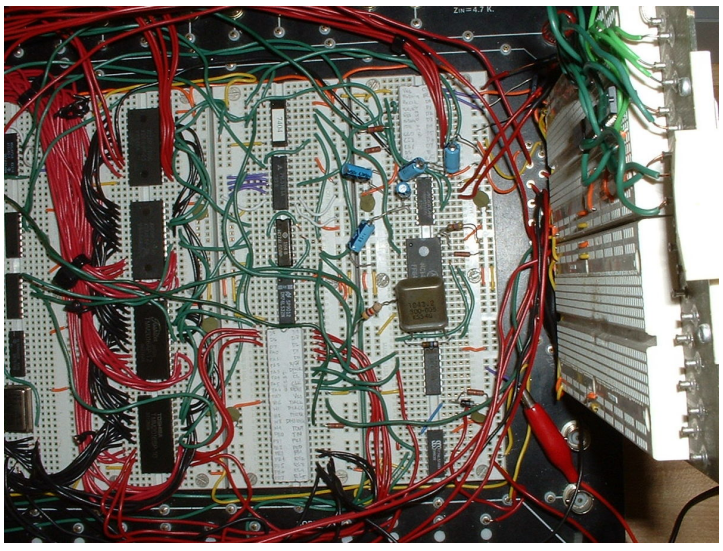
- "GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic" (http://focus.ti.com/lit/an/scea003a/scea003a.pdf), *Application Note* (Texas Instruments), 1997
- *JEDEC Standard JESD8-3A, Gunning Transceiver Logic (GTL) Low-Level, High Speed Interface Standard for Digital Integrated Circuits* (http://www.jedec.org/sites/default/files/docs/JESD8-3A.pdf), JEDEC, May 2007

Transistor–transistor logic

Transistor–transistor logic (**TTL**) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called *transistor–transistor logic* because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors (contrast with RTL and DTL).



A Motorola 68000-based computer with various TTL chips mounted on breadboards.

TTL is notable for being a widespread integrated circuit (IC) family used in many applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, synthesizers, etc. The designation *TTL* is sometimes used to mean TTL-compatible logic levels, even when not associated directly with TTL integrated circuits, for example as a label on the inputs and outputs of electronic instruments.[1]

After their introduction in integrated circuit form in 1963 by Sylvania, TTL integrated circuits were manufactured by several semiconductor companies, with the 7400 series by Texas Instruments becoming particularly popular. TTL

manufacturers offered a wide range of logic gate, flip-flops, counters, and other circuits. Several variations from the original bipolar TTL concept were developed, giving circuits with higher speed or lower power dissipation to allow optimization of a design. TTL circuits simplified design of systems compared to earlier logic families, offering superior speed to resistor–transistor logic (RTL) and easier design layout than emitter-coupled logic (ECL). The design of the input and outputs of TTL gates allowed many elements to be interconnected.

TTL became the foundation of computers and other digital electronics. Even after much larger scale integrated circuits made multiple-circuit-board processors obsolete, TTL devices still found extensive use as the "glue" logic interfacing more densely integrated components. TTL devices were originally made in ceramic and plastic dual-in-line (DIP) packages, and flat-pack form. TTL chips are now also made in surface-mount packages. Successors to the original bipolar TTL logic often are interchangeable in function with the original circuits, but with improved speed or lower power dissipation.

History

TTL was invented in 1961 by James L. Buie of TRW, "particularly suited to the newly developing integrated circuit design technology", and it was originally named *transistor-coupled transistor logic* (TCTL).[2] The first commercial integrated-circuit TTL devices were manufactured by Sylvania in 1963, called the Sylvania Universal High-Level Logic family (SUHL).[3] The Sylvania parts were used in the controls of the Phoenix missile. TTL became popular with electronic systems designers after Texas Instruments introduced the 5400 series of ICs, with military temperature range, in 1964 and the later 7400 series, specified over a narrower range, and with inexpensive plastic packages in 1966.[4]

A real-time clock built of TTL chips around 1979.

The Texas Instruments 7400 family became an industry standard. Compatible parts were made by Motorola, AMD, Fairchild, Intel, Intersil, Signetics, Mullard, Siemens, SGS-Thomson and National Semiconductor,[5][6] and many other companies, even in the Eastern Bloc (Soviet Union, GDR, Poland, Bulgaria).Wikipedia:Citation needed Not only did others make compatible TTL parts, but compatible parts were made using many other circuit technologies as well. At least one manufacturer, IBM, produced non-compatible TTL circuits for its own use; IBM used the technology in the IBM System/38, IBM 4300, and IBM 3081.[7]

The term "TTL" is applied to many successive generations of bipolar logic, with gradual improvements in speed and power consumption over about two decades. The most recently introduced familyWikipedia:Citation needed, 74AS/ALS Advanced Schottky, was introduced in 1985.[8] As of 2008, Texas Instruments continues to supply the more general-purpose chips in numerous obsolete technology families, albeit at increased prices. Typically, TTL chips integrate no more than a few hundred transistors each. Functions within a single package generally range from a few logic gates to a microprocessor bit-slice. TTL also became important because its low cost made digital

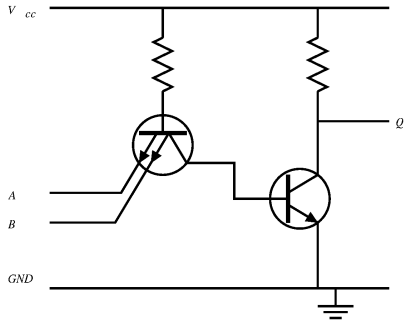
techniques economically practical for tasks previously done by analog methods.[9]

The Kenbak-1, ancestor to the first personal computers, used TTL for its CPU instead of a microprocessor chip, which was not available in 1971.[10] The 1973 Xerox Alto and 1981 Star workstations, which introduced the graphical user interface, used TTL circuits integrated at the level of ALUs and bitslices, respectively. Most computers used TTL-compatible "glue logic" between larger chips well into the 1990s. Until the advent of programmable logic, discrete bipolar logic was used to prototype and emulate microarchitectures under development.

Implementation

Fundamental TTL gate

TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together.[11] The output is buffered by a common emitter amplifier.



Two-input TTL NAND gate with a simple output stage (simplified).

Inputs both logical ones. When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are reverse-biased. Unlike DTL, a small “collector” current (approximately 10μA) is drawn by each of the inputs. This is because the transistor is in reverse-active mode. An approximately constant current flows from the positive rail, through the resistor and into the base of the multiple emitter transistor.[12] This current passes through the base-emitter junction of the output transistor, allowing it to conduct and pulling the output voltage low (logical zero).

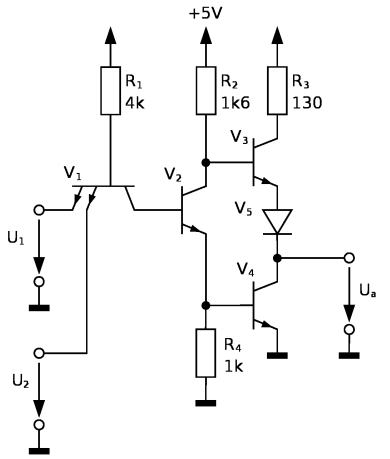
An input logical zero. Note that the base-collector junction of the multiple-emitter transistor and the base-emitter junction of the output transistor are in series between the bottom of the resistor and ground. If one input voltage becomes zero, the corresponding base-emitter junction of the multiple-emitter transistor is in parallel with these two junctions. A phenomenon called current steering means that when two voltage-stable elements with different threshold voltages are connected in parallel, the current flows through the path with the smaller threshold voltage. As a result, no current flows through the base of the output transistor, causing it to stop conducting and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.[13]

The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fanout). Some advantage of the simple output stage is the high voltage level (up to V_{CC}) of the output logical "1" when the output is not loaded.

A common variation omits the collector resistor of the output transistor, making an open collector output. This allows the designer to fabricate logic by connecting the open collector outputs of several logic gates together and providing a single external pull-up resistor. If any of the logic gates becomes logic low (transistor conducting), the combined output will be low. Examples of this type of gate are the 7401[14] and 7403 series.

TTL with a "totem-pole" output stage

To solve the problem with the high output resistance of the simple output stage the second schematic adds to this a "totem-pole" ("push–pull") output. It consists of the two n-p-n transistors V_3 and V_4, the "lifting" diode V_5 and the current-limiting resistor R_3 (see the figure on the right). It is driven by applying the same *current steering* idea as above.



Standard TTL NAND with a "totem-pole" output stage, one of four in 7400

When V_2 is "off", V_4 is "off" as well and V_3 operates in active region as a voltage follower producing high output voltage (logical "1"). When V_2 is "on", it activates V_4, driving low voltage (logical "0") to the output. V_2 and V_4 collector–emitter junctions connect V_4 base–emitter junction in parallel to the series-connected V_3 base–emitter and V_5 anode–cathode junctions. V_3 base current is deprived; the transistor turns "off" and it does not impact on the output. In the middle of the transition, the resistor R_3 limits the current flowing directly through the series connected transistor V_3, diode V_5 and transistor V_4 that are all conducting. It also limits the output current in the case of output logical "1" and short connection to the ground. The strength of the gate may be increased without proportionally affecting the power consumption by removing the pull-up and pull-down resistors from the output stage.[15][16]

The main advantage of TTL with a "totem-pole" output stage is the low output resistance at output logical "1". It is determined by the upper output transistor V_3 operating in active region as a voltage follower. The resistor R_3 does not increase the output resistance since it is connected in the V_3 collector and its influence is compensated by the negative feedback. A disadvantage of the "totem-pole" output stage is the decreased voltage level (no more than 3.5 V) of the output logical "1" (even, if the output is unloaded). The reason of this reduction are the voltage drops across the V_3 base–emitter and V_5 anode–cathode junctions.

Interfacing considerations

Like DTL, TTL is a *current-sinking logic* since a current must be drawn from inputs to bring them to a logic 0 level. At low input voltage, the TTL input sources current which must be absorbed by the previous stage. The maximum value of this current is about 1.6 mA for a standard TTL gate.[17] The input source has to be low-resistive enough (< 500 Ω) so that the flowing current creates only a negligible voltage drop (< 0.8 V) across it, for the input to be considered as a logical "0". TTL inputs are sometimes simply left floating to provide a logical "1", though this usage is not recommended.

Standard TTL circuits operate with a 5-volt power supply. A TTL input signal is defined as "low" when between 0 V and 0.8 V with respect to the ground terminal, and "high" when between 2.2 V and 5 V[18] and if a voltage signal ranges between 0.8 volts and 2 volts were to be sent into the input of a TTL gate, there would be no certain response from the gate and therefore it is considered "uncertain" (precise logic levels vary slightly between sub-types and by temperature). TTL outputs are typically restricted to narrower limits of between 0 V and 0.4 V for a "low" and between 2.6 V and 5 V for a "high", providing 0.4V of noise immunity. Standardization of the TTL levels was so ubiquitous that complex circuit boards often contained TTL chips made by many different manufacturers selected for availability and cost, compatibility being assured; two circuit board units off the same assembly line on different successive days or weeks might have a different mix of brands of chips in the same positions on the board; repair was possible with chips manufactured years (sometimes over a decade) later than original components. Within usefully broad limits, logic gates could be treated as ideal Boolean devices without concern for electrical limitations.

In some cases (e.g., when the output of a TTL logic gate needs to be used for driving the input of a CMOS gate), the voltage level of the "totem-pole" output stage at output logical "1" can be increased up to V_{CC} by connecting an external resistor between the V_3 collector and the positive rail. It pulls up the V_5 cathode and cuts-off the diode.[19] However, this technique actually converts the sophisticated "totem-pole" output into a simple output stage having significant output resistance when driving a high level (determined by the external resistor).

Packaging

Like most integrated circuits of the period 1965–1990, TTL devices are usually packaged in through-hole, dual in-line packages with between 14 and 24 lead wires, usually made of epoxy plastic (PDIP) or sometimes of ceramic (CDIP). Beam-lead chip dice without packages were made for assembly into larger arrays as hybrid integrated circuits. Parts for military and aerospace applications were packaged in flat packs, a form of surface-mount package, with leads suitable for welding or soldering to printed circuit boards. Today, many TTL-compatible devices are available in surface-mount packages, which are available in a wider array of types than through-hole packages.

TTL is particularly well suited to bipolar integrated circuits because additional inputs to a gate merely required additional emitters on a shared base region of the input transistor. If individually packaged transistors were used, the cost of all the transistors would discourage one from using such an input structure. But in an integrated circuit, the additional emitters for extra gate inputs add only a small area.

Comparison with other logic families

Main article: Logic family

TTL devices consume substantially more power than equivalent CMOS devices at rest, but power consumption does not increase with clock speed as rapidly as for CMOS devices.[20] Compared to contemporary ECL circuits, TTL uses less power and has easier design rules but is substantially slower. Designers can combine ECL and TTL devices in the same system to achieve best overall performance and economy, but level-shifting devices are required between the two logic families. TTL is less sensitive to damage from electrostatic discharge than early CMOS devices.

Due to the output structure of TTL devices, the output impedance is asymmetrical between the high and low state, making them unsuitable for driving transmission lines. This drawback is usually overcome by buffering the outputs with special line-driver devices where signals need to be sent through cables. ECL, by virtue of its symmetric low-impedance output structure, does not have this drawback.

The TTL "totem-pole" output structure often has a momentary overlap when both the upper and lower transistors are conducting, resulting in a substantial pulse of current drawn from the power supply. These pulses can couple in unexpected ways between multiple integrated circuit packages, resulting in reduced noise margin and lower performance. TTL systems usually have a decoupling capacitor for every one or two IC packages, so that a current pulse from one TTL chip does not momentarily reduce the supply voltage to another.

Several manufacturers now supply CMOS logic equivalents with TTL-compatible input and output levels, usually bearing part numbers similar to the equivalent TTL component and with the same pinouts. For example, the 74HCT00 series provides many drop-in replacements for bipolar 7400 series parts, but uses CMOS technology.

Sub-types

Successive generations of technology produced compatible parts with improved power consumption or switching speed, or both. Although vendors uniformly marketed these various product lines as TTL with Schottky diodes, some of the underlying circuits, such as used in the LS family, could rather be considered DTL.[21]

Variations of and successors to the basic TTL family, which has a typical gate propagation delay of 10ns and a power dissipation of 10 mW per gate, for a power–delay product (PDP) or switching energy of about 100 pJ, include:

- Low-power TTL (L), which traded switching speed (33ns) for a reduction in power consumption (1 mW) (now essentially replaced by CMOS logic)
- High-speed TTL (H), with faster switching than standard TTL (6ns) but significantly higher power dissipation (22 mW)
- Schottky TTL (S), introduced in 1969, which used Schottky diode clamps at gate inputs to prevent charge storage and improve switching time. These gates operated more quickly (3ns) but had higher power dissipation (19 mW)
- Low-power Schottky TTL (LS) – used the higher resistance values of low-power TTL and the Schottky diodes to provide a good combination of speed (9.5ns) and reduced power consumption (2 mW), and PDP of about 20 pJ. Probably the most common type of TTL, these were used as glue logic in microcomputers, essentially replacing the former H, L, and S sub-families.
- Fast (F) and Advanced-Schottky (AS) variants of LS from Fairchild and TI, respectively, circa 1985, with "Miller-killer" circuits to speed up the low-to-high transition. These families achieved PDPs of 10 pJ and 4 pJ, respectively, the lowest of all the TTL families.
- Low-voltage TTL (LVTTL) for 3.3-volt power supplies and memory interfacing.

Most manufacturers offer commercial and extended temperature ranges: for example Texas Instruments 7400 series parts are rated from 0 to 70 °C, and 5400 series devices over the military-specification temperature range of −55 to +125 °C.

Special quality levels and high-reliability parts are available for military and aerospace applications.

Radiation-hardened devices are offered for space applications.

Applications

Before the advent of VLSI devices, TTL integrated circuits were a standard method of construction for the processors of mini-computer and mainframe processors; such as the DEC VAX and Data General Eclipse, and for equipment such as machine tool numerical controls, printers and video display terminals. As microprocessors became more functional, TTL devices became important for "glue logic" applications, such as fast bus drivers on a motherboard, which tie together the function blocks realized in VLSI elements.

Analog applications

While originally designed to handle logic-level digital signals, a TTL inverter can be biased as an analog amplifier. Connecting a resistor between the output and the input biases the TTL element as a negative feedback amplifier. Such amplifiers may be useful to convert analog signals to the digital domain but would not ordinarily be used where analog amplification is the primary purpose.[22] TTL inverters can also be used in crystal oscillators where their analog amplification ability is significant.

Notes

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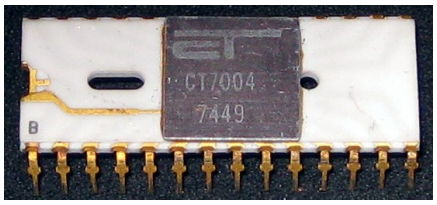
PMOS logic



PMOS Clock IC, 1974

P-type metal-oxide-semiconductor logic uses p-channel metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. PMOS transistors operate by creating an inversion layer in an n-type transistor body. This inversion layer, called p-channel, can conduct holes between p-type "source" and "drain" terminals.

The p-channel is created by applying voltage to the third terminal called gate. Like other MOSFETs, PMOS transistors have four modes of operation: cut-off (or subthreshold), triode, saturation (sometimes called active), and velocity saturation.

The p-type MOSFETs are arranged in a so-called "pull-up network" (PUN) between the logic gate output and positive supply voltage, while a resistor is placed between the logic gate output and the negative supply voltage. The circuit is designed such that if the desired output is high, then the PUN will be active, creating a current path between the positive supply and the output.

While PMOS logic is easy to design and manufacture (a MOSFET can be made to operate as a resistor, so the whole circuit can be made with PMOS FETs), it has several shortcomings as well. The worst problem is that a DC current flows through a PMOS logic gate when the PUN is active, that is whenever the output is high. This leads to static power dissipation even when the circuit sits idle.

Also, PMOS circuits are slow to transition from high to low. When transitioning from low to high, the transistors provide low resistance, and the capacitative charge at the output accumulates very quickly (similar to charging a capacitor through a very low resistor). But the resistance between the output and the negative supply rail is much greater, so the high to low transition takes longer (similar to discharge a capacitor through a high resistor value). Using a resistor of lower value will speed up the process but also increases static power dissipation.

Additionally, the asymmetric input logic levels make PMOS circuits susceptible to noise.

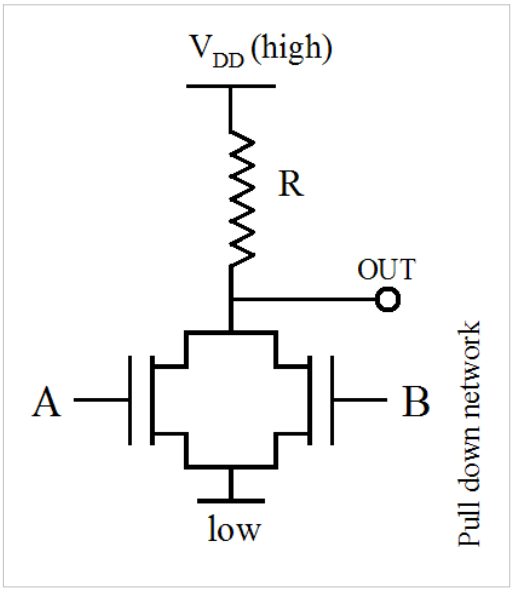
Though initially easier to manufacture, PMOS logic was later supplanted by NMOS logic because NMOS is faster than PMOS. Modern fabs use CMOS, which uses both PMOS and NMOS transistors together. Static CMOS logic leverages the advantages of both by using NMOS and PMOS together in the wafer.

NMOS logic

N-type metal-oxide-semiconductor logic uses n-type metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. NMOS transistors have four modes of operation: cut-off (or sub-threshold), triode, saturation (sometimes called active), and velocity saturation.

The n-type MOSFETs are arranged in a so-called "pull-down network" (PDN) between the logic gate output and negative supply voltage, while a resistor is placed between the logic gate output and the positive supply voltage. The circuit is designed such that if the desired output is low, then the PDN will be active, creating a current path between the negative supply and the output.

As an example, here is a NOR gate in NMOS logic. If either input A or input B is high (logic 1, = True), the respective MOS transistor acts as a very low resistance between the output and the negative supply, forcing the output to be low (logic 0, = False). When both A and B are high, both transistors are conductive, creating an even lower resistance path to ground. The only case where the output is high is when both transistors are off, which occurs only when both A and B are low, thus satisfying the truth table of a NOR gate:



A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

A MOSFET can be made to operate as a resistor, so the whole circuit can be made with n-channel MOSFETs only. For many years, this made NMOS circuits much faster than comparable PMOS and CMOS circuits, which had to use much slower p-channel transistors. It was also easier to manufacture NMOS than CMOS, as the latter has to implement p-channel transistors in special n-wells on the p-substrate. The major problem with NMOS (and most other logic families) is that a DC current must flow through a logic gate even when the output is in a steady state (low in the case of NMOS). This means static power dissipation, i.e. power drain even when the circuit is not switching. This is a similar situation to the modern high speed, high density CMOS circuits (microprocessors etc.) which also has significant static current draw, although this is due to leakage, not bias. However, older and/or slower static CMOS circuits used for ASICs, SRAM etc., typically have very low static power consumption.

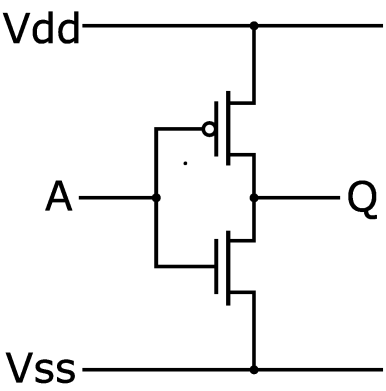
Also, NMOS circuits are slow to transition from low to high. When transitioning from high to low, the transistors provide low resistance, and the capacitative charge at the output drains away very quickly (similar to discharging a capacitor through a very low resistor). But the resistance between the output and the positive supply rail is much greater, so the low to high transition takes longer (similar to charging a capacitor through a high value resistor). Using a resistor of lower value will speed up the process but also increases static power dissipation. However, a better (and the most common) way to make the gates faster is to use depletion-mode transistors instead of enhancement-mode transistors as loads. This is called depletion-load NMOS logic.

Additionally, just like in DTL, TTL and ECL etc., the asymmetric input logic levels make NMOS circuits somewhat susceptible to noise. These disadvantages are why the CMOS logic now has supplanted most of these types in most high-speed digital circuits such as microprocessors (despite the fact that CMOS was originally very slow).

CMOS

For other uses, see CMOS (disambiguation).

Complementary metal–oxide–semiconductor (**CMOS**) /ˈsiːmɒs/ is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858).



CMOS inverter (NOT logic gate)

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS).[1] The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

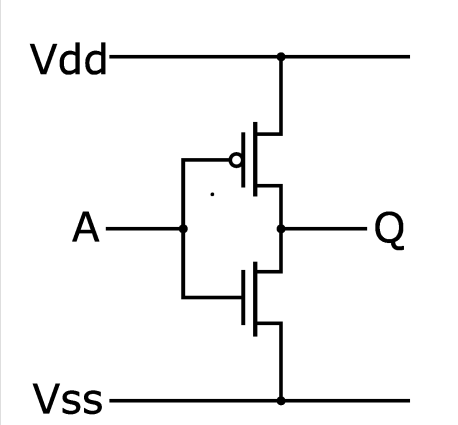
The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.[2]

Technical details

"CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes. As of 2010, CPUs with the best performance per watt each year have been CMOS static logic since 1976.Wikipedia:Citation needed

CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. Although CMOS logic can be implemented with discrete devices for demonstrations, commercial CMOS products are integrated circuits composed of up to billions of transistors of both types, on a rectangular piece of silicon of between 10 and 400 mm^2.

Inversion



Static CMOS Inverter

CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

The image on the right shows what happens when an input is connected to both a PMOS transistor (top of diagram) and an NMOS transistor (bottom of diagram). When the voltage of input A is low, the NMOS transistor's channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output. Because the resistance between the supply voltage and Q is low, the voltage drop between the supply voltage and Q due to a current drawn from Q is small. The output therefore registers a high voltage.

On the other hand, when the voltage of input A is high, the PMOS transistor is in an OFF (high resistance) state so it would limit the current flowing from the positive supply to the output, while the NMOS transistor is in an ON (low resistance) state, allowing the output from drain to ground. Because the resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registering a low voltage.

In short, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behaviour of input and output, the CMOS circuits' output is the inverse of the input.

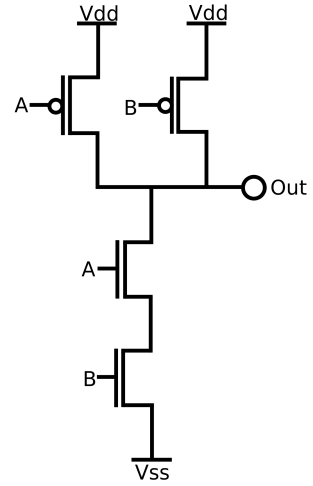
The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground(GND) depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies.[3] These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS.

Duality

An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground. To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground. This can be easily accomplished by defining one in terms of the NOT of the other. Due to the De Morgan's laws based logic, the PMOS transistors in parallel have corresponding NMOS transistors in series while the PMOS transistors in series have corresponding NMOS transistors in parallel.

Logic

More complex logic functions such as those involving AND and OR gates require manipulating the paths between gates to represent the logic. When a path consists of two transistors in series, both transistors must have low resistance to the corresponding supply voltage, modelling an AND. When a path consists of two transistors in parallel, either one or both of the transistors must have low resistance to connect the supply voltage to the output, modelling an OR.



NAND gate in CMOS logic

Shown on the right is a circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and V_{ss} (ground), bringing the output low. If both of the A and B inputs are low, then neither of the NMOS transistors will conduct, while both of the PMOS transistors will conduct, establishing a conductive path between the output and V_{dd} (voltage source), bringing the output high. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and V_{dd} (voltage source), bringing the output high. As the only configuration of the two inputs that results in a low output is when both are high, this circuit implements a NAND (NOT AND) logic gate.

An advantage of CMOS over NMOS is that both low-to-high and high-to-low output transitions are fast since the pull-up transistors have low resistance when switched on, unlike the load resistors in NMOS logic. In addition, the output signal swings the full voltage between the low and high rails. This strong, more nearly symmetric response also makes CMOS more resistant to noise.

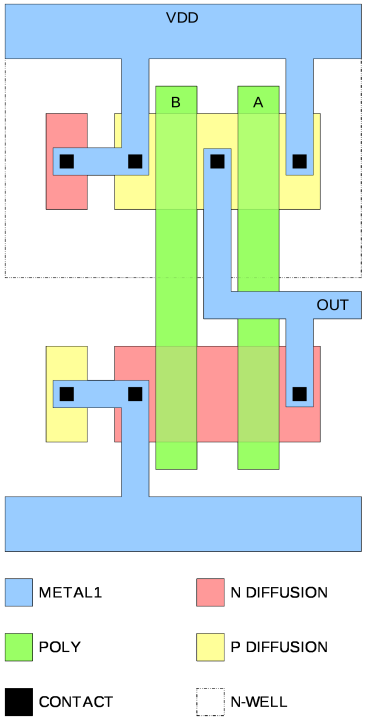
See Logical effort for a method of calculating delay in a CMOS circuit.

Example: NAND gate in physical layout

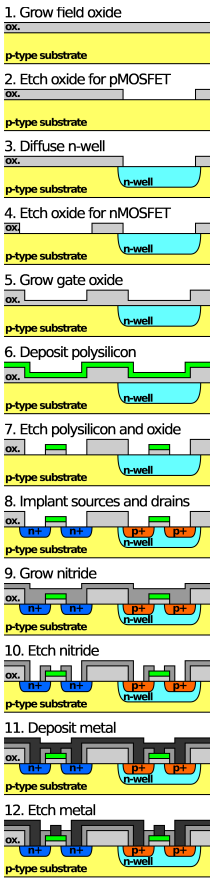
This example shows a NAND logic device drawn as a physical representation as it would be manufactured. The physical layout perspective is a "bird's eye view" of a stack of layers. The circuit is constructed on a P-type substrate. The polysilicon, diffusion, and n-well are referred to as "base layers" and are actually inserted into trenches of the P-type substrate. The contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1) making a connection.

The inputs to the NAND (illustrated in green color) are in polysilicon. The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N diffusion for the N device & P diffusion for the P device (illustrated in salmon and yellow coloring respectively). The output ("out") is connected together in metal (illustrated in cyan coloring). Connections between metal and polysilicon or diffusion are made through contacts (illustrated as black squares). The physical layout example matches the NAND logic circuit given in the previous example.

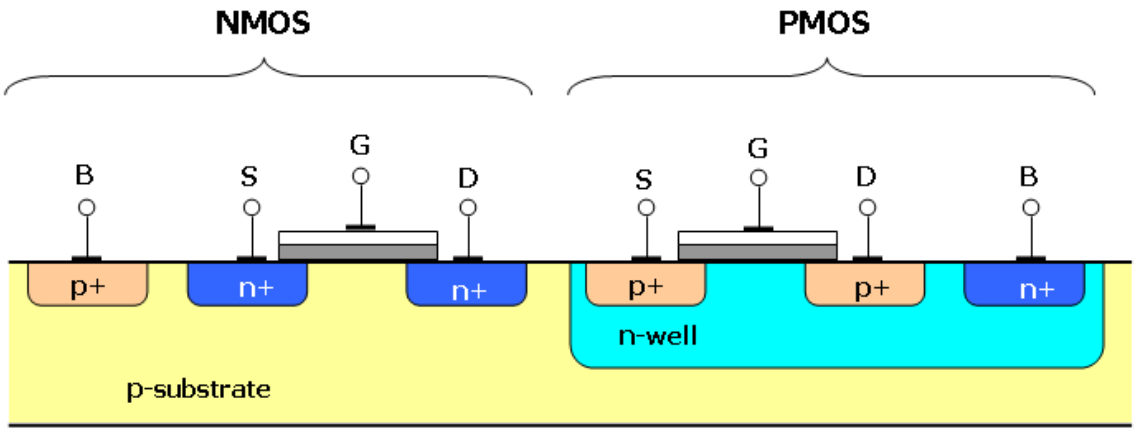
The N device is manufactured on a P-type substrate while the P device is manufactured in an N-type well (n-well). A P-type substrate "tap" is connected to V_{SS} and an N-type n-well tap is connected to V_{DD} to prevent latchup.



The physical layout of a NAND circuit. The larger regions of N-type diffusion and P-type diffusion are part of the transistors. The two smaller regions on the left are taps to prevent latchup.



Simplified process of fabrication of a CMOS inverter on p-type substrate in semiconductor microfabrication. Note: Gate, source and drain contacts are not normally in the same plane in real devices, and the diagram is not to scale.



Cross section of two transistors in a CMOS gate, in an N-well CMOS process

Power: switching and leakage

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). On a typical ASIC in a modern 90 nanometer process, switching the output might take 120 picoseconds, and happens once every ten nanoseconds. NMOS logic dissipates power whenever the transistor is on, because there is a current path from V_{dd} to V_{ss} through the load resistor and the n-type network.

Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously.

Broadly classifying, power dissipation in CMOS circuits occurs because of two components:

Static dissipation

- **Sub threshold conduction when the transistors are off.**

Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called *sub threshold* current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{dd} might have been 5 V, and V_{th} for both NMOS and PMOS might have been 700 mV). A special type of the CMOS transistor with near zero threshold voltage is the native transistor.

- **Tunnelling current through gate oxide.**

SiO_2 is a very good insulator, but at very small thickness levels electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunnelling current becomes very important for transistors below 130 nm technology with gate oxides of 20 Å or thinner.

- **Leakage current through reverse biased diodes.**

Small reverse leakage currents are formed due to formation of reverse bias between diffusion regions and wells (for e.g., p-type diffusion vs. n-well), wells and substrate (for e.g., n-well vs. p-substrate). In modern process diode leakage is very small compared to sub threshold and tunnelling currents, so these may be neglected during power calculations.

- **Contention current in ratioed circuit**

Dynamic Dissipation

- **Charging and discharging of load capacitances.**

CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total of $Q=C_L V_{DD}$ is thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device: $P = CV^2 f$.

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor α, called the activity factor. Now, the dynamic power dissipation may be re-written as $P = \alpha CV^2 f$.

A clock in a system has an activity factor α=1, since it rises and falls every cycle. Most data has an activity factor of 0.1.[4] If correct load capacitance is estimated on a node together with its activity factor, the dynamic power dissipation at that node can be calculated effectively.

- **Short circuit power dissipation**

Since there is a finite rise/fall time for both pMOS and nMOS, during transition, for example, from off to on, both the transistors will be on for a small period of time in which current will find a path directly from V_{DD} to ground, hence creating a short circuit current. Short circuit power dissipation increases with rise and fall time of the transistors.

An additional form of power consumption became significant in the 1990s as wires on chip became narrower and the long wires became more resistive. CMOS gates at the end of those resistive wires see slow input transitions. During the middle of these transitions, both the NMOS and PMOS logic networks are partially conductive, and current flows directly from V_{dd} to V_{SS}. The power thus used is called *crowbar* power. Careful design which avoids weakly driven long skinny wires ameliorates this effect, but crowbar power can be a substantial part of dynamic CMOS power.

To speed up designs, manufacturers have switched to constructions that have lower voltage thresholds but because of this a modern NMOS transistor with a V_{th} of 200 mV has a significant subthreshold leakage current. Designs (e.g. desktop processors) which include vast numbers of circuits which are not actively switching still consume power because of this leakage current. Leakage power is a significant portion of the total power consumed by such designs. Multi-threshold CMOS (MTCMOS), now available from foundries, is one approach to managing leakage power. With MTCMOS, high V_{th} transistors are used when switching speed is not critical, while low V_{th} transistors are used in speed sensitive paths. Further technology advances that use even thinner gate dielectrics have an additional leakage component because of current tunnelling through the extremely thin gate dielectric. Using high-k dielectrics instead of silicon dioxide that is the conventional gate dielectric allows similar device performance, but with a thicker gate insulator, thus avoiding this current. Leakage power reduction using new material and system designs is critical to sustaining scaling of CMOS.[5]

Analog CMOS

Besides digital applications, CMOS technology is also used in analog applications. For example, there are CMOS operational amplifier ICs available in the market. Transmission gates may be used instead of signal relays. CMOS technology is also widely used for RF circuits all the way to microwave frequencies, in mixed-signal (analog+digital) applications.

Temperature range

Conventional CMOS devices work over a range of −55 °C to +125 °C. There were theoretical indications as early as August 2008 that silicon CMOS will work down to −233 °C (40 K).[6] Functioning temperatures near 40 K have since been achieved using overclocked AMD Phenom II processors with a combination of liquid nitrogen and liquid helium cooling.

Single-electron CMOS transistors

Ultra small (L = 20 nm, W = 20 nm) CMOS transistors achieve the single-electron limit when operated at cryogenic temperature over a range of −269 °C (4 K) to about −258 °C (15 K). The transistor displays Coulomb blockade due to progressive charging of electrons one by one. The number of electrons confined in the channel is driven by the gate voltage, starting from an occupation of zero electrons, and it can be set to 1 or many.

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[1] *COS-MOS* was an RCA trademark, which forced other manufacturers to find another name —CMOS

[2] Intel 45nm Hi-k Silicon Technology (http://www.intel.com/technology/45nm/index.htm)

[3] http://www.fairchildsemi.com/an/AN/AN-77.pdf

[4] K. Moiseev, A. Kolodny and S. Wimer, "Timing-aware power-optimal ordering of signals", *ACM Transactions on Design Automation of Electronic Systems*, Volume 13 Issue 4, September 2008, ACM

[5] A good overview of leakage and reduction methods are explained in the book Leakage in Nanometer CMOS Technologies (http://www.springer.com/engineering/circuits+&+systems/book/978-0-387-25737-2) ISBN 0-387-25737-3.

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External links


Wikimedia Commons has media related to ***CMOS***.

- CMOS gate description and interactive illustrations (http://tams-www.informatik.uni-hamburg.de/applets/cmos/)
- LASI (http://lasihomesite.com/) is a "general purpose" IC layout CAD tool. It is a free download and can be used as a layout tool for CMOS circuits.

BiCMOS

'BiCMOS' is an evolved **semiconductor technology** that integrates two formerly separate semiconductor technologies - those of the bipolar junction transistor and the CMOS transistor - in a single integrated circuit device.

Bipolar junction transistors offer high speed, high gain, and low output resistance, which are excellent properties for high-frequency analog amplifiers, whereas CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates. For as long as the two types of transistors have existed in production, designers of circuits utilizing discrete components have realized the advantages of integrating the two technologies; however, lacking implementation in integrated circuits, the application of this free-form design was restricted to fairly simple circuits. Discrete circuits of hundreds or thousands of transistors quickly expand to occupy hundreds or thousands of square centimeters of circuit board area, and for very high-speed circuits such as those used in modern digital computers, the distance between transistors (and the minimum capacitance of the connections between them) also makes the desired speeds grossly unattainable, so that if these designs cannot be built as integrated circuits, then they simply cannot be built.

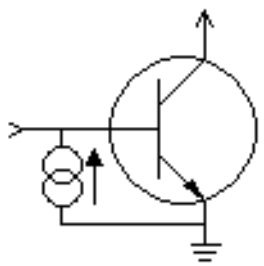
In the 1990s,Wikipedia:Citation needed modern integrated circuit fabrication technologies began to make BiCMOS a reality. This technology rapidly found application in amplifiers and analog power management circuits, and has some advantages in digital logic. BiCMOS circuits use the characteristics of each type of transistor most appropriately. Generally this means that high current circuits use metal–oxide–semiconductor field-effect transistor (MOSFETs) for efficient control, and portions of specialized very high performance circuits use bipolar devices. Examples of this include radio frequency (RF) oscillators, bandgap-based references and low-noise circuits. The Pentium, Pentium Pro, and SuperSPARC microprocessors also used BiCMOS.Wikipedia:Citation needed

Disadvantages

BiCMOS as a fabrication process is not currently as commercially viable for some applications, such as microprocessors, as with exclusively BJT or CMOS fabrication. Unfortunately, many of the advantages of CMOS fabrication, for example, do not transfer directly to BiCMOS fabrication. An inherent difficulty arises from the fact that optimizing both the BJT and MOS components of the process is impossible without adding many extra fabrication steps and consequently increasing the process cost. Finally, in the area of high performance logic, BiCMOS may never offer the (relatively) low power consumption of CMOS alone, due to the potential for higher standby leakage current. An exclusive mix of BiCMOS and CMOS has appeal if the performance attributes of each type of gate can be optimized. But since CMOS is already ideal for pure digital logic, this is only a serious issue when it is desirable to put logic circuits together on the same chip with other circuits that are not strictly logic: either for the purpose of a mixed-signal application, or simply to reduce the chip count in an electronic product by combining two chips into one, in order to reduce cost, size, and/or weight.

Integrated injection logic

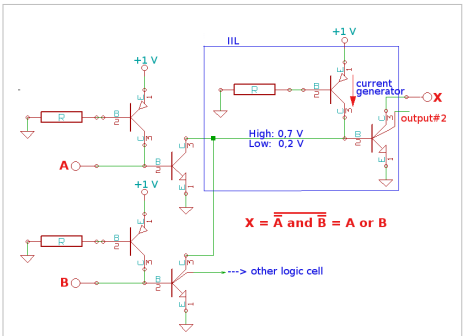
Integrated injection logic (**IIL**, **I^2L**, or **I2L**) is a class of digital circuits built with multiple collector bipolar junction transistors (BJT). When introduced it had speed comparable to TTL yet was almost as low power as CMOS, making it ideal for use in VLSI (and larger) integrated circuits. Although the logic voltage levels are very close (High: 0.7V, Low: 0.2V), I2L has high noise immunity because it operates by current instead of voltage. Sometimes also known as Merged Transistor Logic.



Simplified schematic of an I2L inverter.

Operation

The heart of an I2L circuit is the common emitter open collector inverter. Typically, an inverter consists of an NPN transistor with the emitter connected to ground and the base biased with a forward current. The input is supplied to the base as either a current sink (low logic level) or as a high-z floating condition (high logic level). The output of an inverter is at the collector. Likewise, it is either a current sink (low logic level) or a high-z floating condition (high logic level).



IIL circuit

Like direct-coupled transistor logic, there is no resistor between the output (collector) of one NPN transistor and the input (base) of the following transistor.

To understand how the inverter operates, it is necessary to understand the current flow. If the bias current is shunted to ground (low logic level), the transistor turns off and the collector floats (high logic level). If the bias current is not shunted to ground because the input is high-z (high logic level), the bias current flows through the transistor to the emitter, switching on the transistor, and allowing the collector to sink current (low logic level). Because the output of the inverter can sink current but cannot source current, it is safe to connect the outputs of multiple inverters together to form a wired AND gate. When the outputs of two inverters are wired together, the result is a two-input NOR gate because the configuration (NOT A) AND (NOT B) is equivalent to NOT (A OR B). This logical relationship is known as De Morgan's Theorem.

Usage

I2L is relatively simple to construct on an integrated circuit, and was commonly used before the advent of CMOS logic by companies such as Motorola (now Freescale) and Texas Instruments. In 1975, Sinclair Radionics introduced one of the first consumer-grade digital watches, the Black Watch, which used I2L technology. In 1979, HP introduced a frequency measurement instrument based on a HP-made custom LSI chip that uses integrated injection logic (I2L) for low power consumption and high density, enabling portable battery operation, and also some emitter function logic (EFL) circuits where high speed is needed.[1]

Generally, I2L gates were constructed with transistors with 1, 2 or 3 separate collectors. This fan-out of up to 3 allowed 3-input NAND or NOR gates to be constructed very simply with just a single layer of interconnect metal.

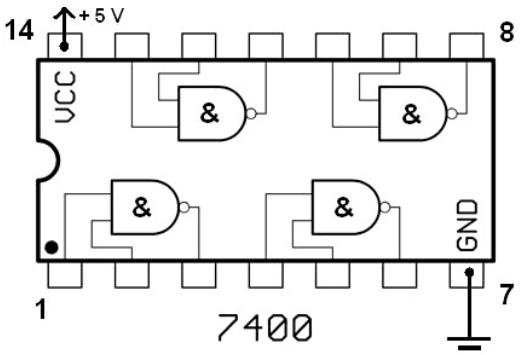
RCA used I²L in late 1970s in its CA3162 ADC 3 digit meter.

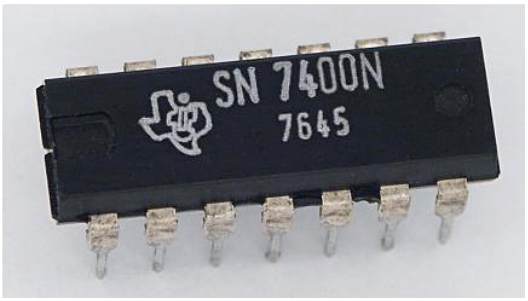
References

[1] "HP memory project: Time, Frequency Standard & Counter" (http://www.hpmemory.org/wb_pages/wall_b_page_01.htm)

7400 series

The **7400 series** of transistor–transistor logic (TTL) integrated circuits are the most popular family of TTL integrated circuit logic.[2][3] Quickly replacing diode–transistor logic, it was used to build the mini and mainframe computers of the 1960s and 1970s. Several generations of pin-compatible descendants of the original family have since become *de facto* standard electronic components.





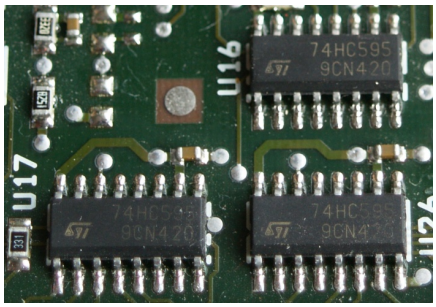
The 7400 chip, containing four NANDs. The second line of numbers (7645) is a date code; this chip was manufactured in the 45th week of 1976.[1] The N suffix on the part number is a vendor-specific code indicating PDIP packaging.

Overview

The 7400 series contains hundreds of devices that provide everything from basic logic gates, flip-flops, and counters, to special purpose bus transceivers and arithmetic logic units (ALU). Specific functions are described in a list of 7400 series integrated circuits.

Today, surface-mounted CMOS versions of the 7400 series are used in various applications in electronics and for glue logic in computers and industrial electronics. The original through-hole devices in dual in-line packages (DIP/DIL), which were the mainstay of the industry for many decades, are very useful for rapid breadboard-prototyping and education and so remain available from most manufacturers. The fastest types and very low voltage versions are typically surface-mount only, however.

The first part number in the series, the 7400, designates a device containing four two-input NAND gates. Each gate uses two pins for input and one pin for its output, and the remaining two contacts supply power (+5 V) and connect the ground. This part was made in various packages including flat pack, plastic or ceramic dual in-line packages with 14 pins, and in surface mount packages as well. Additional numbers and letters in a full part number identify the package and other variations.



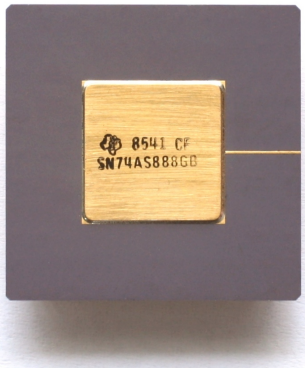
Surface-mounted 74HC595 shift registers on a PCB

While designed as a family of digital logic, some TTL chips were used in analog circuits like Schmitt triggers. Like the 4000 series, the newer CMOS versions of the 7400 series are also usable as analog amplifiers using negative feedback (similar to operational amplifiers with only an inverting input).

The former Soviet Union manufactured the K155ЛА3 which was pin-compatible with the 7400 part available in the United States, except for using a metric spacing of 2.5mm between pins instead of the 1/10"-based (2.54mm) spacing used in the west.

7400 series derivative families

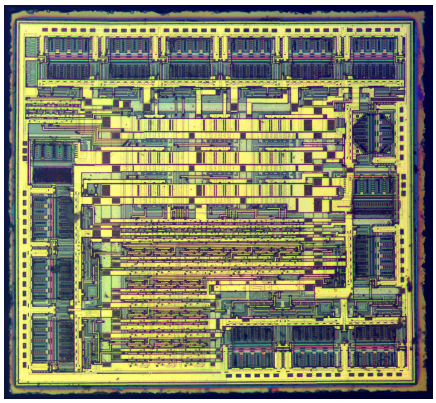
7400 series parts were constructed using bipolar transistors, forming what is referred to as transistor–transistor logic or **TTL**. Newer series, more or less compatible in function and logic level with the original parts, use CMOS technology or a combination of the two (BiCMOS). Originally the bipolar circuits provided higher speed but consumed more power than the competing 4000 series of CMOS devices. Bipolar devices are also limited to a fixed power supply voltage, typically 5 V, while CMOS parts often support a range of supply voltages.



Part of the 7400 series: cascadable 8-bit ALU Texas Instruments SN74AS888

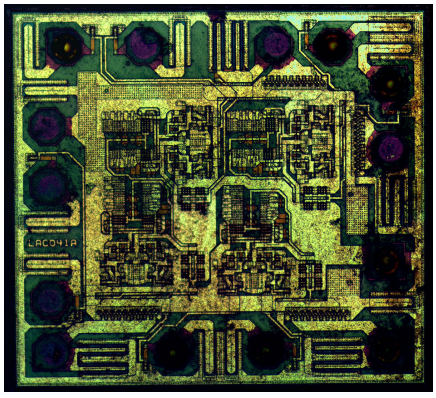
Milspec-rated devices for use in extended temperature conditions are available as the 5400 series. Texas Instruments also manufactured radiation-hardened devices with the prefix *RSN*, and the company offered beam-lead bare dies for integration into hybrid circuits with a *BL* prefix designation.

Regular-speed TTL parts were also available for a time in the 6400 series – these had an extended industrial temperature range of −40 °C to +85 °C. While companies such as Mullard listed 6400-series compatible parts in 1970 data sheets,[4] by 1973 there was no mention of the 6400 family in the Texas Instruments *TTL Data Book*. Some companies have also offered industrial extended temperature range variants using the regular 7400 series part numbers with a prefix or suffix to indicate the temperature grade.


Die of a 74HC595 8-bit shift register

As integrated circuits in the 7400 series were made in different technologies, usually compatibility was retained with the original TTL logic levels and power supply voltages. An integrated circuit made in CMOS is not a TTL chip, since it uses field-effect transistors (FETs) and not bipolar junction transistors, but similar part numbers are retained to identify similar logic functions and electrical (power and I/O voltage) compatibility in the different subfamilies. Over 40 different logic subfamilies use this standardized part number scheme.[5]

- Bipolar
  - 74 – Standard TTL. the original logic family had no letters between the "74" and the part number. 10 ns gate delay, 10 mW dissipation, 4.75–5.25 V, released in 1966.[6]
  - 74L – Low-power. Larger resistors allowed 1 mW dissipation at the cost of a very slow 33 ns gate delay. Obsolete, replaced by 74LS or CMOS technology. Introduced 1971.[7]
  - 74H – High-speed. 6 ns gate delay but 22 mW power dissipation. Used in 1970s era supercomputers. Still produced but generally superseded by the 74S series. Introduced in 1971.


Die of a 74AHC00D quad 2-input NAND gate manufactured by NXP Semiconductors

- 74S – High-speed Schottky. Implemented with Schottky diode clamps at the inputs to prevent charge storage, this provides faster operation than the 74 and 74H series at the cost of increased power consumption and cost. 3 ns gate delay, 20 mW dissipation, released in 1971.
- 74LS – Low-power Schottky. Implemented using the same technology as 74S but with reduced power consumption and switching speed. Typical 10 ns gate delay, a remarkable (for the time) 2 mW dissipation, 4.75–5.25 V.
- 74AS – Advanced Schottky, the next iteration of the 74S series with greater speed and fan-out despite lower power consumption. Implemented using the 74S's technology with "miller killer" circuitry to speed up the low-to-high transition. 1.7 ns gate delay, 8 mW, 4.5–5.5 V.
- 74ALS – Advanced low-power Schottky. Same technology as 74AS but with the speed/power tradeoff of the 74LS. 4 ns, 1.2 mW, 4.5–5.5 V.
- 74F – Fast. Fairchild's version of TI's 74AS. 3.4 ns, 6 mW, 4.5–5.5 V. Introduced in 1978.

- CMOS
  - C – CMOS 4–15 V operation similar to buffered 4000 (4000B) series.
  - HC – High-speed CMOS, similar performance to LS, 12 ns. 2.0–6.0 V.
  - HCT – High speed, compatible logic levels to bipolar parts.
  - AC – Advanced CMOS, performance generally between S and F.
  - ACQ – Advanced CMOS with Quiet outputs.
  - AHC – Advanced high-speed CMOS, three times as fast as HC.
  - ALVC – Low-voltage – 1.8–3.3 V, time Propagation Delay (TPD) < 3 ns at 3.3 V.
  - ALVT – Low-voltage – 2.5–3.3 V, 5 V tolerant inputs, high current ≤ 64 mA, TPD < 3 ns at 2.5 V.
  - AUC – Low-voltage – 0.8–2.5 V, TPD < 2.5 ns at 1.8 V.
  - AUP – Low-voltage – 0.8–3.6 V (3.3 V typically), TPD 15.6/8.2/4.3 ns at 1.2/1.8/3.3V, partial power-down specified (IOFF), inputs protected.
  - AVC – Low-voltage – 1.8–3.3 V, TPD < 3.2 ns at 1.8 V, bus hold, IOFF.
  - FC – Fast CMOS, performance similar to F.
  - LCX – CMOS with 3 V supply and 5 V tolerant inputs.
  - LV – Low-voltage CMOS – 2.0–5.5 V supply and 5 V tolerant inputs.
  - LVC – Low voltage – 1.65–3.3 V and 5 V tolerant inputs, TPD < 5.5 ns at 3.3 V, TPD < 9 ns at 2.5 V.
  - LV-A – 2.5–5 V, 5 V tolerant inputs, TPD < 10 ns at 3.3 V, bus hold, IOFF, low noise.
  - LVT – Low-voltage – 3.3 V supply, 5 V tolerant inputs, high output current < 64 mA, TPD < 3.5 ns at 3.3 V, IOFF, low noise.
  - LVQ – Low-voltage – 3.3 V.
  - LVX – Low-voltage – 3.3 V with 5 V tolerant inputs.
  - VHC – Very-high-speed CMOS – "S" performance in CMOS technology and power.
- BiCMOS
  - BCT – BiCMOS, TTL-compatible input thresholds, used for buffers.
  - ABT – Advanced BiCMOS, TTL-compatible input thresholds, faster than ACT and BCT.

Many parts in the CMOS HC, AC, and FC families are also offered in "T" versions (HCT, ACT, and FCT) which have input thresholds that are compatible with both TTL and 3.3 V CMOS signals. The non-T parts have conventional CMOS input thresholds.

The 74H family is the same basic design as the 7400 family with resistor values reduced. This reduced the typical propagation delay from 9 ns to 6 ns but increased the power consumption. The 74H family provided a number of unique devices for CPU designs in the 1970s. Many designers of military and aerospace equipment used this family over a long period and as they need exact replacements, this family is still produced by Lansdale Semiconductor.[8]

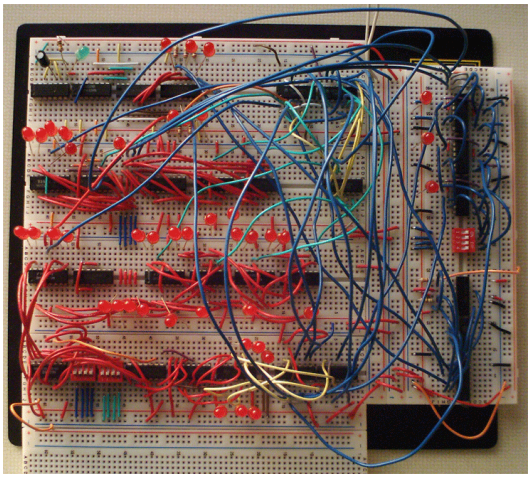
The 74S family, using Schottky circuitry, uses more power than the 74, but is faster. The 74LS family of ICs is a lower-power version of the 74S family, with slightly higher speed but lower power dissipation than the original 74 family; it became the most popular variant once it was widely available.

The 74F family was introduced by Fairchild Semiconductor and adopted by other manufacturers; it is faster than the 74, 74LS and 74S families.

Through the late 1980s and 1990s newer versions of this family were introduced to support the lower operating voltages used in newer CPU devices.

History

Although the 7400 series was the first *de facto* industry standard TTL logic family (i.e. second-sourced by several semiconductor companies), there were earlier TTL logic families such as the Sylvania SUHL (Sylvania Universal High-level Logic) family, Motorola MC4000 MTTL family (not to be confused with RCA CD4000 CMOS), the National Semiconductor DM8000 family, Fairchild 9300 series, and the Signetics 8200 family.



A 4-bit, 2 register, six-instruction computer made entirely of 74-series chips

The 7400N quad NAND gate was the first product in the series, introduced by Texas Instruments in a military grade metal flat package in October 1964. The extremely popular commercial grade plastic DIP followed in the third quarter of 1966.[9]

The 5400 and 7400 series were used in many popular minicomputers in the 1970s and early 1980s. The DEC PDP series 'minis' used the 74181 ALU as the main computing element in the CPU. Other examples were the Data General Nova series and Hewlett-Packard 21MX, 1000, and 3000 series.

Hobbyists and students equipped with wire wrap tools, a 'breadboard' and a 5-volt power supply could also experiment with digital logic referring to how-to articles in *Byte* magazine and *Popular Electronics* which featured circuit examples in nearly every issue. In the early days of large-scale IC development, a prototype of a new large-scale integrated circuit might have been developed using TTL chips on several circuit boards, before committing to manufacture of the target device in IC form. This allowed simulation of the finished product and testing of the logic before the availability of software simulations of integrated circuits.

In 1965, typical quantity-one pricing for the SN5400 (military grade, in ceramic welded flat-pack) was around 22 USD. As of 2007, individual commercial-grade chips in molded epoxy (plastic) packages can be purchased for approximately 0.25 USD each, depending on the particular chip.

Part numbering scheme

The part numbers for 7400 series logic devices often use the following naming convention, though specifics vary between manufacturers.

- First, although sometimes omitted, a two or three letter prefix which indicates the manufacturer of the device (e.g. SN for Texas Instruments, DM for National Semiconductor) although these codes are no longer closely associated with a single manufacturer, for example Fairchild Semiconductor manufactures parts with MM and DM prefixes, and none.

- Two digits, where "74" indicates a commercial temperature range device and "54" indicates a military temperature range. Historically: "64" indicated a short lived series with an intermediate "industrial" temperature range.
- Up to four letters describing the logic subfamily, as listed above (e.g. "LS" or "HCT").
- Two or more digits assigned for each device, e.g. 00 for a quad 2-input NAND gate. There are hundreds of different devices in each family. The allocation of device numbers (and, with a few exceptions, the pin-outs) of the original 7400 family was carried across to the later families, and new numbers allocated for new functions, plus some of the competing CD4000 numbers and pin-outs were included over time. There is no pattern to the allocation of these numbers. The function and pin-out of the chip is nearly always the same for the same device number regardless of subfamily manufacturer – exceptions are discussed below.
- Additional suffix letters and numbers may be attached to indicate the package type, quality grade, or other information, but this varies widely by manufacturer.

For example **SN74ALS245N** means this is a device probably made by Texas Instruments (SN), it is a commercial temperature range TTL device (74), it is a member of the "advanced low-power Schottky" family (ALS), and it is a *bi-directional eight-bit buffer* (245) in a plastic through-hole DIP package (N).

Many logic families maintain a consistent use of the device numbers, as an aid to designers. Often a part from a different 74x00 subfamily could be substituted ("drop-in replacement") in a circuit, with the same function and pin-out yet more appropriate characteristics for an application (perhaps speed or power consumption), which was a large part of the appeal of the 74C00 series over the competing CD4000B series, for example. But there are a few exceptions where incompatibilities (mainly in pin-out) across the subfamilies occurred, such as:

- some flat-pack devices (e.g. 7400W) and surface-mount devices,
- some of the faster CMOS series (for example 74AC),
- a few low-power TTL devices (e.g. 74L86, 74L9 and 74L95) have a different pin-out than the regular (or even 74LS) series part.
- five versions of the 74x54 (4-wide AND-OR-INVERT gates IC), namely 7454(N), 7454W, 74H54, 74L54W and 74L54N/74LS54, are different from each other in pin-out and/or function,

Second sources in Europe and the Eastern Bloc

Some manufacturers such as Mullard and Siemens had pin-compatible TTL parts but with a completely different numbering scheme, however, data sheets identified the *7400-compatible* number as an aid to recognition.

At the time the 7400 series was being made, some European manufacturers (that traditionally followed the Pro Electron naming convention) such as Philips/Mullard produced a series of TTL integrated circuits with part names beginning FJ. Some examples of FJ series are:

- FJH101 (=7430) Single 8-input NAND gate,
- FJH131 (=7400) Quadruple 2-input NAND gate,
- FJH181 (=7454N or J) 2+2+2+2 input AND-OR-NOT gate.

The Soviet Union started manufacturing TTL ICs with 7400 series pin-out in the late 1960s and early 1970s. Part numbering is different from the Western series:

- the technology modifications were considered different series, and were identified by different numbered prefixes – 155 series is equivalent to plain 74, 131 series is 74H, 158 series is 74L, 531 series is 74S, 555 series is 74LS, and 1530/1531/1533 are 74F/74AS/74ALS respectively. CMOS elements with TTL pin-out are also available, for example 1564 series is equivalent to 74HC.
- the function of the unit is described with a two-letter code followed by a number
  - the first letter represents the functional group – logical, triggers, counters, multiplexers, etc.

- the second letter shows the functional subgroup making the distinction between logical NAND and NOR, D- and JK-triggers, decimal and binary counters, etc.
- the number distinguishes variants with different number of inputs, or different number of elements within a die – ЛА1/ЛА2/ЛА3 (LA1/LA2/LA3) are 2 four-input / 1 eight-input / 4 two-input NAND elements respectively (equivalent to 7420/7430/7400)

Before July 1974 the two letters from the functional description were inserted after the first digit of the series. Examples: К1ЛБ551 and К155ЛА1 (7420), К1ТМ552 and К155ТМ2 (7474) are the same ICs made at different times.

Clones of the plain 7400 series were also made in other Eastern Bloc countries[10]

- Poland and Czechoslovakia used the 7400 numbering scheme with manufacturer prefixes UCY and MH respectively. Examples: UCY7400, and MH7400.
- Hungary also used the 7400 numbering scheme but with manufacturer suffix – 7400 is marked as 7400APC.
- Romania used trimmed 7400 numbering with own manufacturing prefix CDB. Example: CDB4123E is 74123.
- East Germany also used trimmed 7400 numbering without manufacturer prefix or suffix. The prefix D (or E) designates digital IC, and not the manufacturer. Example: D174 is 7474. 74LS clones were designated by the prefix DL; e.g. DL000 = 74LS00. In later years East German made clones were also available with standard 74* numbers, usually for export.[11]

No information is available for technology modifications (74H, 74LS, etc.) manufactured outside USSR.

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[1] http://homepages.nildram.co.uk/~wylie/ICs/monolith.htm The first monolithic integrated circuits, retrieved 2013 December 7

[2] http://www.computerhistory.org/semiconductor/timeline/1963-TTL.html The Computer History Museum, 1963 Standard Logic Families Introduced, retrieved 2008 April 16

[3] Don Lancaster, "TTL Cookbook", Howard W. Sams and Co., Indianapolis, 1975, ISBN 0-672-21035-5 , preface

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[5] "Logic reference guide: Bipolar, BiCMOS, and CMOS Logic Technology" (http://focus.ti.com/lit/ml/scyb004b/scyb004b.pdf)

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[8] Lansdale Semiconductor home page (http://www.lansdale.com)

[9] http://smithsonianchips.si.edu/texas/ic.htm

[10] http://www.pchelar-probvaisambg.com/statia115_40_spisak.htm

[11] GDR semiconductor datasheet comparison (http://www-user.tu-chemnitz.de/~heha/bastelecke/KonsumgÃ¼ter-Bastelei/DDR-Halbleiter/#d) (in German)

List of 7400 series integrated circuits

The following is a **list of 7400 series digital logic integrated circuits**. The SN7400 series originated with TTL integrated circuits made by Texas Instruments. Because of the popularity of these parts, they were second-sourced by other manufacturers who kept the 7400 sequence number as an aid to identification of compatible parts. As well, compatible TTL parts originated by other manufacturers were second sourced in the TI product line under a 74xxx series part number.

Just the *base numbers* are listed below, that is: parts are listed here as if made in the basic, standard power and speed, TTL form, although many later parts were never manufactured with that technology.

Part number	Description	Datasheet
7400	quad 2-input NAND gate	HC/HCT [1]
741G00	single 2-input NAND gate	
7401	quad 2-input NAND gate with open collector outputs	
741G01	single 2-input NAND gate with open drain output	
7402	quad 2-input NOR gate	HC/HCT [2]
741G02	single 2-input NOR gate	
7403	quad 2-input NAND gate with open collector outputs	HC/HCT [3]
741G03	single 2-input NAND gate with open drain output	
7404	hex inverter	HC/HCT [4]
741G04	single inverter	
7405	hex inverter with open collector outputs	HC [5]
741G05	single inverter with open drain output	
7406	hex inverter buffer/driver with 30 V open collector outputs	
741G06	single inverting buffer/driver with open drain output	
7407	hex buffer/driver with 30 V open collector outputs	
741G07	single non-inverting buffer/driver with open drain output	
7408	quad 2-input AND gate	HC/HCT [6]
741G08	single 2-input AND gate	
7409	quad 2-input AND gate with open collector outputs	
741G09	single 2-input AND gate with open drain output	
7410	triple 3-input NAND gate	HC/HCT [7]
7411	triple 3-input AND gate	HC/HCT [8]
7412	triple 3-input NAND gate with open collector outputs	
7413	dual Schmitt trigger 4-input NAND gate	
7414	hex Schmitt trigger inverter	HC/HCT [9]
741G14	single Schmitt trigger inverter	
7415	triple 3-input AND gate with open collector outputs	

7416	hex inverter buffer/driver with 15 V open collector outputs	
7417	hex buffer/driver with 15 V open collector outputs	
741G17	single Schmitt-trigger buffer	
7418	dual 4-input NAND gate with Schmitt trigger inputs	
7419	hex Schmitt trigger inverter	
7420	dual 4-input NAND gate	HC/HCT [10]
7421	dual 4-input AND gate	HC [11]
7422	dual 4-input NAND gate with open collector outputs	
7423	expandable dual 4-input NOR gate with strobe	
7424	quad 2-input NAND gate gates with schmitt-trigger line-receiver inputs.	
7425	dual 4-input NOR gate with strobe	
7426	quad 2-input NAND gate with 15 V open collector outputs	
7427	triple 3-input NOR gate	HC/HCT [12]
741G27	single 3-input NOR gate	
7428	quad 2-input NOR buffer	
7430	8-input NAND gate	HC/HCT [13]
7431	hex delay elements	
7432	quad 2-input OR gate	HC/HCT [14]
741G32	single 2-input OR gate	
7433	quad 2-input NOR buffer with open collector outputs	
7434	hex noninverters	
7435	hex noninverters with open-collector outputs	
7436	quad 2-input NOR gate (different pinout than 7402)	
7437	quad 2-input NAND buffer	
7438	quad 2-input NAND buffer with open collector outputs	
7439	quad 2-input NAND buffer with open collector outputs, input and output terminals flipped, otherwise functionally identical to 7438	
7440	dual 4-input NAND buffer	
7441	BCD to decimal decoder/Nixie tube driver	
7442	BCD to decimal decoder	HC/HCT [15]
7443	excess-3 to decimal decoder	
7444	excess-3-Gray code to decimal decoder	
7445	BCD to decimal decoder/driver	
7446	BCD to seven-segment display decoder/driver with 30 V open collector outputs	
7447	BCD to 7-segment decoder/driver with 15 V open collector outputs	
7448	BCD to 7-segment decoder/driver with Internal Pullups	
7449	BCD to 7-segment decoder/driver with open collector outputs	
7450	dual 2-wide 2-input AND-OR-invert gate (one gate expandable)	

7451	dual 2-wide 2-input AND-OR-invert gate	
7452	expandable 4-wide 2-input AND-OR gate	
7453	expandable 4-wide 2-input AND-OR-invert gate	
7454	3-2-2-3-input AND-OR-invert gate	
7455	2-wide 4-input AND-OR-invert Gate (74H version is expandable)	
7456	50:1 frequency divider	
7457	60:1 frequency divider	
7458	2-input & 3-input AND-OR Gate	HC/HCT [16]
7459	2-input & 3-input AND-OR-invert Gate	
7460	dual 4-input expander	
7461	triple 3-input expander	
7462	3-2-2-3-input AND-OR expander	
7463	hex current sensing interface gates	
7464	4-2-3-2-input AND-OR-invert gate	
7465	4-2-3-2 input AND-OR-invert gate with open collector output	
7468	dual 4 bit decade counters	
7469	dual 4 bit binary counters	
7470	AND-gated positive edge triggered J-K flip-flop with preset and clear	
74H71	AND-or-gated J-K master-slave flip-flop with preset	
74L71	AND-gated R-S master-slave flip-flop with preset and clear	
7472	AND gated J-K master-slave flip-flop with preset and clear	
7473	dual J-K flip-flop with clear	HC [17]
7474	dual D positive edge triggered flip-flop with preset and clear	HC/HCT [18]
7475	4-bit bistable latch	HC [19]
7476	dual J-K flip-flop with preset and clear	
7477	4-bit bistable latch	
74H78	dual positive pulse triggered J-K flip-flop with preset, common clock, and common clear	
74L78	dual positive pulse triggered J-K flip-flop with preset, common clock, and common clear	
74Ls78	dual negative edge triggered J-K flip-flop with preset, common clock, and common clear	
7479	dual D flip-flop	
741G79	single D-type flip-flop positive edge trigger non-inverting output	
7480	gated full adder	
741G80	single D-type flip-flop positive edge trigger inverting output	
7481	16-bit random access memory	
7482	2-bit binary full adder	
7483	4-bit binary full adder	
7484	16-bit random access memory	
7485	4-bit magnitude comparator	HC/HCT [20]

7486	quad 2-input XOR gate	HC/HCT [21]
741G86	single 2 input exclusive-OR gate	
7487	4-bit true/complement/zero/one element	
7488	256-bit read-only memory	
7489	64-bit random access memory	
7490	decade counter (separate divide-by-2 and divide-by-5 sections)	
7491	8-bit shift register, serial In, serial out, gated input	
7492	divide-by-12 counter (separate divide-by-2 and divide-by-6 sections)	
7493	4-bit binary counter (separate divide-by-2 and divide-by-8 sections)	HC/HCT [22]
7494	4-bit shift register, dual asynchronous presets	
7495	4-bit shift register, parallel In, parallel out, serial input	
7496	5-bit parallel-In/parallel-out shift register, asynchronous preset	
7497	synchronous 6-bit binary rate multiplier	
741G97	configurable multiple-function gate	
7498	4-bit data selector/storage register	
7499	4-bit bidirectional universal shift register	
74100	dual 4-bit bistable latch	
74101	AND-OR-gated J-K negative-edge-triggered flip-flop with preset	
74102	AND-gated J-K negative-edge-triggered flip-flop with preset and clear	
74103	dual J-K negative-edge-triggered flip-flop with clear	
74104	J-K master-slave flip-flop	
74105	J-K master-slave flip-flop	
74106	dual J-K negative-edge-triggered flip-flop with preset and clear	
74107	dual J-K flip-flop with clear	HC/HCT [23]
74107a	dual J-K negative-edge-triggered flip-flop with clear	
74108	dual J-K negative-edge-triggered flip-flop with preset, common clear, and common clock	
74109	dual J-Not-K positive-edge-triggered flip-flop with clear and preset	HC/HCT [24]
74110	AND-gated J-K master-slave flip-flop with data lockout	
74111	dual J-K master-slave flip-flop with data lockout	
74112	dual J-K negative-edge-triggered flip-flop with clear and preset	HC/HCT [25]
74113	dual J-K negative-edge-triggered flip-flop with preset	
74114	dual J-K negative-edge-triggered flip-flop with preset, common clock and clear	
74116	dual 4-bit latch with clear	
74118	hex set/reset latch	
74119	hex set/reset latch	
74120	dual pulse synchronizer/drivers	
74121	monostable multivibrator	
74122	retriggerable monostable multivibrator with clear	HC/HCT [26]

74123	dual retriggerable monostable multivibrator with clear	HC/HCT [26]
741G123	single retriggerable monostable multivibrator with clear	
74124	dual voltage-controlled oscillator	
74125	quad bus buffer with three-state outputs, negative enable	HC/HCT [27]
741G125	buffer/Line driver, three-state output with active low output enable	
74126	quad bus buffer with three-state outputs, positive enable	HC/HCT [28]
741G126	buffer/line driver, three-state output with active high output enable	
74128	quad 2-input NOR Line driver	
74130	quad 2-input AND gate buffer with 30 V open collector outputs	
74131	quad 2-input AND gate buffer with 15 V open collector outputs	
74132	quad 2-input NAND schmitt trigger	HC/HCT [29]
74133	13-input NAND gate	
74134	12-input NAND gate with three-state output	
74135	quad exclusive-or/NOR gate	
74136	quad 2-input XOR gate with open collector outputs	
74137	3 to 8-line decoder/demultiplexer with address latch	HC [30]
74138	3 to 8-line decoder/demultiplexer	HC/HCT [31]
74139	dual 2 to 4-line decoder/demultiplexer	HC/HCT [32]
74140	dual 4-input NAND line driver	
74141	BCD to decimal decoder/driver for cold-cathode indicator/Nixie tube	
74142	decade counter/latch/decoder/driver for Nixie tubes	
74143	decade counter/latch/decoder/7-segment driver, 15 ma constant current	
74144	decade counter/latch/decoder/7-segment driver, 15 V open collector outputs	
74145	BCD to decimal decoder/driver	
74147	10-line to 4-line priority encoder	HC/HCT [33]
74148	8-line to 3-line priority encoder	
74150	16-line to 1-line data selector/multiplexer	
74151	8-line to 1-line data selector/multiplexer	HC/HCT [34]
74152	8-line to 1-line data selector/multiplexer	
74153	dual 4-line to 1-line data selector/multiplexer	HC/HCT [35]
74154	4-line to 16-line decoder/demultiplexer	HC/HCT [36]
74155	dual 2-line to 4-line decoder/demultiplexer	
74156	dual 2-line to 4-line decoder/demultiplexer with open collector outputs	
74157	quad 2-line to 1-line data selector/multiplexer, noninverting	HC/HCT [37]
74158	quad 2-line to 1-line data selector/multiplexer, inverting	HC [38]
74159	4-line to 16-line decoder/demultiplexer with open collector outputs	

74160	synchronous 4-bit decade counter with asynchronous clear	HC/HCT [39]
74161	synchronous 4-bit binary counter with asynchronous clear	HC/HCT [40]
74162	synchronous 4-bit decade counter with synchronous clear	HC/HCT [41]
74163	synchronous 4-bit binary counter with synchronous clear	HC/HCT [42]
74164	8-bit parallel-out serial shift register with asynchronous clear	HC/HCT [43]
74165	8-bit serial shift register, parallel Load, complementary outputs	HC/HCT [44]
74166	parallel-Load 8-bit shift register	HC/HCT [45]
74167	synchronous decade rate multiplier	
74168	synchronous 4-bit up/down decade counter	
74169	synchronous 4-bit up/down binary counter	
74170	4 by 4 register file with open collector outputs	
74171	quad D-type flip-flops with clear	
74172	16-bit multiple port register file with three-state outputs	
74173	quad d flip-flop with three-state outputs	HC/HCT [46]
74174	hex d flip-flop with common clear	HC/HCT [47]
74175	quad d edge-triggered flip-flop with complementary outputs and asynchronous clear	HC/HCT [48]
74176	presettable decade (bi-quinary) counter/latch	
74177	presettable binary counter/latch	
74178	4-bit parallel-access shift register	
74179	4-bit parallel-access shift register with asynchronous clear and complementary Q_d outputs	
74180	9-bit odd/even parity bit generator and checker	
74181	4-bit arithmetic logic unit and function generator	
74182	lookahead carry generator	
74183	dual carry-save full adder	
74184	BCD to binary converter	
74185	6-bit binary to BCD converter	
74186	512-bit (64x8) read-only memory with open collector outputs	
74187	1024-bit (256x4) read only memory with open collector outputs	
74188	256-bit (32x8) programmable read-only memory with open collector outputs	
74189	64-bit (16x4) RAM with inverting three-state outputs	F [49]
74190	synchronous up/down decade counter	
74191	synchronous up/down binary counter	HC/HCT [50]
74192	synchronous up/down decade counter with clear	
74193	synchronous up/down 4-bit binary counter with clear	HC/HCT [51]
74194	4-bit bidirectional universal shift register	HC/HCT [52]
74195	4-bit parallel-access shift register	

74196	presettable decade counter/latch	
74197	presettable binary counter/latch	
74198	8-bit bidirectional universal shift register	
74199	8-bit bidirectional universal shift register with J-Not-K serial inputs	
74200	256-bit ram with three-state outputs	
74201	256-bit (256x1) ram with three-state outputs	
74206	256-bit ram with open collector outputs	
74209	1024-bit (1024x1) ram with three-state output	
74210	octal buffer	
74219	64-bit (16x4) RAM with noninverting three-state outputs	
74221	dual monostable multivibrator with schmitt trigger input	HC/HCT [53]
74222	16 by 4 synchronous FIFO memory with three-state outputs	
74224	16 by 4 synchronous FIFO memory with three-state outputs	
74225	asynchronous 16x5 FIFO memory	
74226	4-bit parallel latched bus transceiver with three-state outputs	
74227	64-bit fifo memories 16x4	
74228	64-bit fifo memories 16x4 open-collector outputs	
74230	octal buffer/driver with three-state outputs, true and complementary inputs	
74231	octal buffer and line driver with three-state outputs, G and /G complementary inputs	
74232	quad NOR Schmitt trigger	
74237	3-of-8 decoder/demultiplexer with address latch, active high outputs	HC [54]
74238	3-of-8 decoder/demultiplexer, active high outputs	HC/HCT [55]
74239	dual 2-of-4 decoder/demultiplexer, active high outputs	
74240	octal buffer with Inverted three-state outputs	HC/HCT [56]
74241	octal buffer with noninverted three-state outputs	HC/HCT [57]
74242	quad bus transceiver with Inverted three-state outputs	
74243	quad bus transceiver with noninverted three-state outputs	HC [58]
74244	octal buffer with noninverted three-state outputs	HC/HCT [59]
74245	octal bus transceiver with noninverted three-state outputs	HC/HCT [60]
74246	BCD to 7-segment decoder/driver with 30 V open collector outputs	
74247	BCD to 7-segment decoder/driver with 15 V open collector outputs	
74248	BCD to 7-segment decoder/driver with Internal Pull-up outputs	
74249	BCD to 7-segment decoder/driver with open collector outputs	
74250	1 of 16 data selectors/multiplexers	
74251	8-line to 1-line data selector/multiplexer with complementary three-state outputs	HC/HCT [61]
74253	dual 4-line to 1-line data selector/multiplexer with three-state outputs	HC/HCT [62]
74255	dual 4-bit addressable latch	

74256	dual 4-bit addressable latch	
74257	quad 2-line to 1-line data selector/multiplexer with noninverted three-state outputs	HC/HCT [63]
74258	quad 2-line to 1-line data selector/multiplexer with Inverted three-state outputs	HC [64]
74259	8-bit addressable latch	HC/HCT [65]
74260	dual 5-input NOR gate	
74261	2-bit by 4-bit parallel binary multiplier	
74264	look ahead carry generator	
74265	quad complementary output elements	
74266	quad 2-input XNOR gate with open collector outputs	
74268	hex d-type latches three-state outputs, common output control, common enable	
74270	2048-bit (512x4) read only memory with open collector outputs	
74271	2048-bit (256x8) read only memory with open collector outputs	
74273	8-bit register with reset	HC/HCT [66]
74274	4-bit by 4-bit binary multiplier	
74275	7-bit slice Wallace tree	
74276	quad J-Not-K edge-triggered Flip-Flops with separate clocks, common preset and clear	
74278	4-bit cascadeable priority registers with latched data inputs	
74279	quad set-reset latch	
74280	9-bit odd/even Parity bit Generator/checker	HC/HCT [67]
74281	4-bit parallel binary accumulator	
74282	look-ahead carry generator with selectable carry inputs	
74283	4-bit binary Full adder	HC [68]
74284	4-bit by 4-bit parallel binary multiplier (low order 4 bits of product)	
74285	4-bit by 4-bit parallel binary multiplier (high order 4 bits of product)	
74286	9-bit parity generator/checker with bus driver parity I/O port	
74287	1024-bit (256x4) programmable read-only memory with three-state outputs	
74288	256-bit (32x8) programmable read-only memory with three-state outputs	
74289	64-bit (16x4) RAM with open collector outputs	
74290	decade counter (separate divide-by-2 and divide-by-5 sections)	
74291	4-bit universal shift register, binary up/down counter, synchronous	
74292	programmable frequency divider/digital timer	
74293	4-bit binary counter (separate divide-by-2 and divide-by-8 sections)	
74294	programmable frequency divider/digital timer	
74295	4-bit bidirectional register with three-state outputs	
74297	digital phase-locked-loop filter	
74298	quad 2-input multiplexer with storage	
74299	8-bit bidirectional universal shift/storage register with three-state outputs	HC/HCT [69]
74301	256-bit (256x1) random access memory with open collector output	

74309	1024-bit (1024x1) random access memory with open collector output	
74310	octal buffer with Schmitt trigger inputs	
74314	1024-bit random access memory	
74319	64-bit random access memories 16x4 open collector outputs	
74320	crystal controlled oscillator	
74321	crystal-controlled oscillators with F/2 and F/4 count-down outputs	
74322	8-bit shift register with sign extend, three-state outputs	
74323	8-bit bidirectional universal shift/storage register with three-state outputs	
74324	voltage controlled oscillator (or crystal controlled)	
74340	octal buffer with Schmitt trigger inputs and three-state inverted outputs	
74341	octal buffer with Schmitt trigger inputs and three-state noninverted outputs	
74344	octal buffer with Schmitt trigger inputs and three-state noninverted outputs	
74347	bcd to seven segment decoders/drivers open collector outputs, low voltage version of 7447	
74348	8 to 3-line priority encoder with three-state outputs	
74350	4-bit shifter with three-state outputs	
74351	dual 8-line to 1-line data selectors/multiplexers with three-state outputs and 4 common data inputs	
74352	dual 4-line to 1-line data selectors/multiplexers with inverting outputs	
74353	dual 4-line to 1-line data selectors/multiplexers with inverting three-state outputs	
74354	8 to 1-line data selector/multiplexer with transparent latch, three-state outputs	
74355	8-line to 1-line data selector/multiplexer with transparent registers, open-collector outputs	
74356	8 to 1-line data selector/multiplexer with edge-triggered register, three-state outputs	
74357	8-line to 1-line data selectors/multiplexers/edge-triggered registers, open-collector outputs	
74361	bubble memory function timing generator	
74362	four-phase clock generator/driver	
74363	octal three-state D-latches	
74365	hex buffer with noninverted three-state outputs	HC/HCT [70]
74366	hex buffer with Inverted three-state outputs	HC/HCT [71]
74367	hex buffer with noninverted three-state outputs	HC/HCT [72]
74368	hex buffer with Inverted three-state outputs	HC/HCT [73]
74370	2048-bit (512x4) read-only memory with three-state outputs	
74371	2048-bit (256x8) read-only memory with three-state outputs	
74373	octal transparent latch with three-state outputs	HC/HCT [74]
741G373	single transparent latch with three-state output	
74374	octal register with three-state outputs	HC/HCT [75]
741G374	single d-type flip-flop with three-state output	
74375	quad bistable latch	
74376	quad J-Not-K flip-flop with common clock and common clear	
74377	8-bit register with clock enable	HC/HCT [76]

74378	6-bit register with clock enable	
74379	4-bit register with clock enable and complementary outputs	
74380	8-bit multifunction register	
74381	4-bit arithmetic logic unit/function generator with generate and propagate outputs	
74382	4-bit arithmetic logic unit/function generator with ripple carry and overflow outputs	
74384	8-bit by 1-bit two's complement multipliers	
74385	quad 4-bit adder/subtractor	
74386	quad 2-input XOR gate	
74387	1024-bit (256x4) programmable read-only memory with open collector outputs	
74388	4-bit register with standard and three-state outputs	
74390	dual 4-bit decade counter	HC/HCT [77]
74393	dual 4-bit binary counter	HC/HCT [78]
74395	4-bit universal shift register with three-state outputs	
74396	octal storage registers, parallel access	
74398	quad 2-input multiplexers with storage and complementary outputs	
74399	quad 2-input multiplexer with storage	
74405	1 to 8 decoder, equivalent to Intel 8205, only found as UCY74S405 so might be non-TI number	
74408	8-bit parity tree	
74412	multi-mode buffered 8-bit latches with three-state outputs and clear	
74422	re-triggerable mono-stable multivibrators, two inputs	
74423	dual retriggerable monostable multivibrator	HC/HCT [79]
74424	two-phase clock generator/driver	
74425	quad gates with three-state outputs and active low enables	
74426	quad gates with three-state outputs and active high enables	
74428	system controller for 8080a	
74436	line driver/memory driver circuits - mos memory interface, damping output resistor	
74437	line driver/memory driver circuits - mos memory interface	
74438	system controller for 8080a	
74440	quad tridirectional bus transceiver with noninverted open collector outputs	
74441	quad tridirectional bus transceiver with Inverted open collector outputs	
74442	quad tridirectional bus transceiver with noninverted three-state outputs	
74443	quad tridirectional bus transceiver with Inverted three-state outputs	
74444	quad tridirectional bus transceiver with Inverted and noninverted three-state outputs	
74445	bcd-to-decimal decoders/drivers	
74446	quad bus transceivers with direction controls	
74447	bcd-to-seven-segment decoders/drivers, low voltage version of 74247	
74448	quad tridirectional bus transceiver with Inverted and noninverted open collector outputs	
74449	quad bus transceivers with direction controls, true outputs	
74450	16-to-1 multiplexer with complementary outputs	

74451	dual 8-to-1 multiplexer	
74452	dual decade counter, synchronous	
74453	dual binary counter, synchronous	
74453	quad 4-to-1 multiplexer	
74454	dual decade up/down counter, synchronous, preset input	
74455	dual binary up/down counter, synchronous, preset input	
74456	NBCD (Natural binary coded decimal) adder	
74460	bus transfer switch	
74461	8-bit presettable binary counter with three-state outputs	
74462	fiber-optic link transmitter	
74463	fiber-optic link receiver	
74465	octal buffer with three-state true outputs	
74466	octal buffers with three-state inverted outputs	
74467	octal buffers with three-state true outputs	
74468	octal buffers with three-state inverted outputs	
74470	2048-bit (256x8) programmable read-only memory with open collector outputs	
74471	2048-bit (256x8) programmable read-only memory with three-state outputs	
74472	programmable read-only memory with open collector outputs	
74473	programmable read-only memory with three-state outputs	
74474	programmable read-only memory with open collector outputs	
74475	programmable read-only memory with three-state outputs	
74481	4-bit slice cascadable processor elements	
74482	4-bit slice expandable control elements	
74484	BCD-to-binary converter	
74485	binary-to-BCD converter	
74490	dual decade counter	
74491	10-bit binary up/down counter with limited preset and three-state outputs	
74498	8-bit bidirectional shift register with parallel inputs and three-state outputs	
74508	8-bit multiplier/divider	
74518	8-bit comparator with open collector output, input pull-up resistor	
74519	8-bit comparator with open collector output	
74520	8-bit comparator with inverted totem-pole output, input pull-up resistor	
74521	8-bit comparator with inverted totem-pole output	
74522	8-bit comparator with inverted open-collector output, input pull-up resistor	
74526	fuse programmable identity comparator, 16 bit	
74527	fuse programmable identity comparator, 8 bit + 4 bit conventional Identity comparator	
74528	fuse programmable Identity comparator, 12 bit	
74531	octal transparent latch with 32 ma three-state outputs	
74532	octal register with 32 ma three-state outputs	

74533	octal transparent latch with inverting three-state outputs	
74534	octal register with inverting three-state outputs	HCT [80]
74535	octal transparent latch with inverting three-state outputs	
74536	octal register with inverting 32 ma three-state outputs	
74537	BCD to decimal decoder with three-state outputs	
74538	1 of 8 decoder with three-state outputs	
74539	dual 1 of 4 decoder with three-state outputs	
74540	inverting octal buffer with three-state outputs	HC/HCT [81]
74541	non-inverting octal buffer with three-state outputs	HC/HCT [82]
74544	non-inverting octal registered transceiver with three-state outputs	
74558	8-bit by 8-bit multiplier with three-state outputs	
74560	4-bit decade counter with three-state outputs	
74561	4-bit binary counter with three-state outputs	
74563	8-bit d-type transparent latch with inverting three-state outputs	HC/HCT [83]
74564	8-bit d-type edge-triggered register with inverting three-state outputs	HC [84]
74568	decade up/down counter with three-state outputs	
74569	binary up/down counter with three-state outputs	
74573	octal D-type transparent latch with three-state outputs	HC/HCT [85]
74574	octal D-type edge-triggered flip-flop with three-state outputs	HC/HCT [86]
74575	octal D-type flip-flop with synchronous clear, three-state outputs	
74576	octal D-type flip-flop with inverting three-state outputs	
74577	octal D-type flip-flop with synchronous clear, inverting three-state outputs	
74580	octal transceiver/latch with inverting three-state outputs	
74589	8-bit shift register with input latch, three-state outputs	
74590	8-bit binary counter with output registers and three-state outputs	HC [87]
74591	8-bit binary counters with output registers, open-collector outputs	
74592	8-bit binary counter with input registers	
74593	8-bit binary counter with input registers and three-state outputs	
74594	8-bit shift registers with output latches	HC/HCT [88]
74595	8-bit shift registers with output latches, three-state parallel outputs	HC/HCT [89]
74596	8-bit shift registers with output latches, open-collector parallel outputs	
74597	8-bit shift registers with input latches	HC/HCT [90]
74598	8-bit shift register with input latches	
74599	8-bit shift registers with output latches, open-collector outputs	
74600	dynamic memory refresh controller, transparent and burst modes, for 4K or 16K drams	
74601	dynamic memory refresh controller, transparent and burst modes, for 64K drams	
74602	dynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K drams	

74603	dynamic memory refresh controller, cycle steal and burst modes, for 64K drams	
74604	octal 2-input multiplexer with latch, high-speed, with three-state outputs	
74605	latch, high-speed, with open collector outputs	
74606	octal 2-input multiplexer with latch, glitch-free, with three-state outputs	
74607	octal 2-input multiplexer with latch, glitch-free, with open collector outputs	
74608	memory cycle controller	
74610	memory mapper, latched, three-state outputs	
74611	memory mapper, latched, open collector outputs	
74612	memory mapper, three-state outputs	
74613	memory mapper, open collector outputs	
74618	Schmitt-trigger positive-nand gates with totem-pole outputs	
74619	Schmitt-trigger inverters with totem-pole outputs	
74620	octal bus transceiver, inverting, three-state outputs	
74621	octal bus transceiver, noninverting, open collector outputs	
74622	octal bus transceiver, inverting, open collector outputs	
74623	octal bus transceiver, noninverting, three-state outputs	
74624	voltage-controlled oscillator with enable control, range control, two-phase outputs	
74625	dual voltage-controlled oscillator with two-phase outputs	
74626	dual voltage-controlled oscillator with enable control, two-phase outputs	
74627	dual voltage-controlled oscillator	
74628	voltage-controlled oscillator with enable control, range control, external temperature compensation, and two-phase outputs	
74629	dual voltage-controlled oscillator with enable control, range control	
74630	16-bit error detection and correction (EDAC) with three-state outputs	
74631	16-bit error detection and correction with open collector outputs	
74632	32-bit parallel error detection and correction, three-state outputs, byte-write	
74633	32-bit parallel error detection and correction, open-collector outputs, byte-write	
74634	32-bit parallel error detection and correction, three-state outputs	
74635	32-bit parallel error detection and correction, open-collector outputs	
74638	octal bus transceiver with inverting three-state outputs	
74639	octal bus transceiver with noninverting three-state outputs	
74640	octal bus transceiver with inverting three-state outputs	HC/HCT [91]
74641	octal bus transceiver with noninverting open collector outputs	
74642	octal bus transceiver with inverting open collector outputs	
74643	octal bus transceiver with mix of inverting and noninverting three-state outputs	
74644	octal bus transceiver with mix of inverting and noninverting open collector outputs	
74645	octal bus transceiver	
74646	octal bus transceiver/latch/multiplexer with noninverting three-state outputs	
74647	octal bus transceiver/latch/multiplexer with noninverting open collector outputs	

74648	octal bus transceiver/latch/multiplexer with inverting three-state outputs	
74649	octal bus transceiver/latch/multiplexer with inverting open collector outputs	
74651	octal bus transceiver/register with inverting three-state outputs	
74652	octal bus transceiver/register with noninverting three-state outputs	HC/HCT [92]
74653	octal bus transceiver/register with inverting three-state and open collector outputs	
74654	octal bus transceiver/register with noninverting three-state and open collector outputs	
74658	octal bus transceiver with Parity, inverting	
74659	octal bus transceiver with Parity, noninverting	
74664	octal bus transceiver with Parity, inverting	
74665	octal bus transceiver with Parity, noninverting	
74668	synchronous 4-bit decade Up/down counter	
74669	synchronous 4-bit binary Up/down counter	
74670	4 by 4 register File with three-state outputs	HC/HCT [93]
74671	4-bit bidirectional shift register/latch /multiplexer with three-state outputs	
74672	4-bit bidirectional shift register/latch/multiplexer with three-state outputs	
74673	16-bit serial-in serial-out shift register with output storage registers, three-state outputs	
74674	16-bit parallel-in serial-out shift register with three-state outputs	
74677	16-bit address comparator with enable	
74678	16-bit address comparator with latch	
74679	12-bit address comparator with latch	
74680	12-bit address comparator with enable	
74681	4-bit parallel binary accumulator	
74682	8-bit magnitude comparator	
74683	8-bit magnitude comparator with open collector outputs	
74684	8-bit magnitude comparator	
74685	8-bit magnitude comparator with open collector outputs	
74686	8-bit magnitude comparator with enable	
74687	8-bit magnitude comparator with enable	
74688	8-bit equality comparator	HC/HCT [94]
74689	8-bit magnitude comparator with open collector outputs	
74690	three-state outputs	
74691	4-bit binary counter/latch/multiplexer with asynchronous reset, three-state outputs	
74692	4-bit decimal counter/latch/multiplexer with synchronous reset, three-state outputs	
74693	4-bit binary counter/latch/multiplexer with synchronous reset, three-state outputs	
74694	4-bit decimal counter/latch/multiplexer with synchronous and asynchronous resets, three-state outputs	
74695	4-bit binary counter/latch/multiplexer with synchronous and asynchronous resets, three-state outputs	
74696	4-bit decimal counter/register/multiplexer with asynchronous reset, three-state outputs	
74697	4-bit binary counter/register/multiplexer with asynchronous reset, three-state outputs	
74698	4-bit decimal counter/register/multiplexer with synchronous reset, three-state outputs	

74699	4-bit binary counter/register/multiplexer with synchronous reset, three-state outputs	
74716	programmable decade counter	
74718	programmable binary counter	
74724	voltage controlled multivibrator	
74740	octal buffer/Line driver, inverting, three-state outputs	
74741	octal buffer/Line driver, noninverting, three-state outputs, mixed enable polarity	
74744	octal buffer/Line driver, noninverting, three-state outputs	
74748	8 to 3-line priority encoder	
74779	8-bit bidirectional binary counter (three-state)	
74783	synchronous address multiplexer	
74790	error detection and correction (EDAC)	
74794	8-bit register with readback	
74795	octal buffer with three-state outputs	
74796	octal buffer with three-state outputs	
74797	octal buffer with three-state outputs	
74798	octal buffer with three-state outputs	
74804	hex 2-input NAND drivers	
74805	hex 2-input NOR drivers	
74808	hex 2-input AND drivers	
74822	10-bit bus interface flipflop with three-state outputs	
74832	hex 2-input OR drivers	
74848	8 to 3-line priority encoder with three-state outputs	
74873	octal transparent latch	
74874	octal d-type flip-flop	
74876	octal d-type flip-flop with inverting outputs	
74878	dual 4-bit d-type flip-flop with synchronous clear, noninverting three-state outputs	
74879	dual 4-bit d-type flip-flop with synchronous clear, inverting three-state outputs	
74880	octal transparent latchwith inverting outputs	
74881	arithmetic logic unit	
74882	32-bit lookahead carry generator	
74888	8-bit slice processor	
74901	hex inverting TTL buffer	
74902	hex non-inverting TTL buffer	
74903	hex inverting CMOS buffer	
74904	hex non-inverting CMOS buffer	
74905	12-Bit successive approximation register	
74906	hex open drain n-channel buffers	
74907	hex open drain p-channel buffers	
74908	dual CMOS 30 V relay driver	

74909	quad voltage comparator	
74910	256x1 CMOS static RAM	
74911	4 digit expandable display controller	
74912	6 digit BCD display controller and driver	
74914	hex schmitt trigger with extended input voltage	
74915	seven segment to BCD decoder	
74917	6 digit Hex display controller and driver	
74918	dual CMOS 30 V relay driver	
74920	256x4 CMOS static RAM	
74921	256x4 CMOS static RAM	
74922	16-key encoder	
74923	20-key encoder	
74925	4-digit counter/display driver	
74926	4-digit counter/display driver	
74927	4-digit counter/display driver	
74928	4-digit counter/display driver	
74929	1024x1 CMOS static RAM	
74930	1024x1 CMOS static RAM	
74932	phase comparator	
74933	address bus comparator	
74934	=ADC0829 ADC, see corresponding NSC datasheet	
74935	3.5-digit digital voltmeter (DVM) support chip for multiplexed 7-segment displays	
74936	3.75-digit digital voltmeter (DVM) support chip for multiplexed 7-segment displays	
74937	=ADC3511 ADC, see corresponding NSC datasheet	
74938	=ADC3711 ADC, see corresponding NSC datasheet	
74941	octal bus/line drivers/line receivers	
74945	4 digit up/down counter with decoder and driver	
74947	4 digit up/down counter with decoder and driver	
74948	=ADC0816 ADC, see corresponding NSC datasheet	
74949	=ADC0808 ADC, see corresponding NSC datasheet	
741005	hex inverting buffer with open-collector output	
741035	hex noninverting buffers with open-collector outputs	
742960	error detection and correction (EDAC)	
742961	edac bus buffer, inverting	
742962	edac bus buffer, noninverting	
742968	dynamic memory controller	
742969	memory timing controller for use with EDAC	
742970	memory timing controller for use without EDAC	
741G3208	single 3 input OR-AND Gate;	

744002	dual 4-input NOR gate	HC/HCT [95]
744015	dual 4-bit shift registers	HC/HCT [96]
744016	quad bilateral switch	HC/HCT [97]
744017	5-stage ÷10 Johnson counter	HC/HCT [98]
744020	14-stage binary counter	HC/HCT [99]
744024	7 stage ripple carry binary counter	HC [100]
744028	BCD to decimal decoder	
744040	12-stage binary ripple counter	HC/HCT [101]
744046	phase-locked loop and voltage-controlled oscillator	HC/HCT [102]
744049	hex inverting buffer	HC [103]
744050	hex buffer/converter (non-inverting)	HC [104]
744051	high-speed CMOS 8-channel analog multiplexer/demultiplexer	HC/HCT [105]
744052	dual 4-channel analog multiplexer/demultiplexers	HC/HCT [106]
744053	triple 2-channel analog multiplexer/demultiplexers	HC/HCT [107]
744059	programmable divide-by-N counter	HC/HCT [108]
744060	14-stage binary ripple counter with oscillator	HC/HCT [109]
744066	quad bilateral switches	HC/HCT [110]
744067	16-channel analog multiplexer/demultiplexer	HC/HCT [111]
744075	triple 3-input OR gate	HC/HCT [112]
744078	8-input OR/NOR gate	
744094	8-bit three-state shift register/latch	HC/HCT [113]
744316	quad analog switch	HC/HCT [114]
744351	8-channel analog multiplexer/demultiplexer with latch	HC/HCT [115]
744353	Triple 2-channel analog multiplexer/demultiplexer with latch	HC/HCT [116]

744511	BCD to 7-segment decoder	HC/HCT [117]
744514	4-to-16 line decoder/demultiplexer with input latches	HC/HCT [118]
744520	dual 4-bit synchronous binary counter	HC/HCT [119]
744538	dual retriggerable precision monostable multivibrator	HC/HCT [120]
747007	hex buffer	
747266	quad 2-input XNOR gate	HC [121]
7429841	10-bit bus-interface D-type latch with three-state outputs	
7440103	presettable 8-bit synchronous down counter	HC [122]
7440105	4-bit by 16-word FIFO register	HC/HCT [123]

Notes

Some TTL logic parts were made with an extended military-specification temperature range. These parts are prefixed with **54** instead of **74** in the part number. A short-lived **64** prefix on Texas Instruments parts indicated an industrial temperature range; this prefix had been dropped from the TI literature by 1973. Most recent 7400 series parts are fabricated in CMOS or BiCMOS technology rather than TTL. Surface mount parts with a single gate (often in a 5-pin or 6-pin package) are prefixed with **741G** instead of **74**.

Some manufacturers released some 4000 equivalent CMOS circuits with a 74 prefix, for example the 74HC4066 was a replacement for the 4066 with slightly different electrical characteristics (different power supply voltage ratings, higher frequency capabilities, lower "on" resistances in analog switches, etc.). See list of 4000 series integrated circuits.

Conversely, the 4000 series has "borrowed" from the 7400 series - such as the CD40193 and CD40161 being pin-for-pin *functional* replacements for 74C193 and 74C161. There is some reference to double-borrowings, such as 74193 -> 40193 -> 74HC40193.[124]

Older TTL parts made by manufacturers such as Signetics, Motorola, Mullard and Siemens may have different numeric prefix and numbering series entirely, such as in the European FJ family FJH101 is an 8-input NAND gate like a 7430.

A few alphabetic characters to designate a specific logic subfamily may immediately follow the **74** or **54** in the part number, e.g., 74LS74 for Low-power Schottky. Some CMOS parts such as 74HCT74 for High-speed CMOS with TTL-compatible input thresholds are functionally similar to the TTL part. Not all functions are available in all families.

In a few instances, such as the 7478 and 74107, the same suffix in different families do not have completely equivalent logic functions.

Another extension to the series is the **7416xxx** variant, representing mostly the 16-bit wide counterpart of otherwise 8-bit-wide "base" chips with the same three ending digits. Thus e.g. a "7416373" would be the 16-bit-wide equivalent of a "74373". Some 7416xxx parts, however, do not have a direct counterpart from the standard 74xxx range but deliver new functionality instead, which needs making use of the 7416xxx series' higher pin count. For more details, refer primarily to the Texas Instruments documentation mentioned in the References section.

For CMOS (HC, HCT, etc.) subfamilies, read "open drain" for "open collector" in the above table.

There are a few numeric suffixes that have multiple conflicting assignments, such as the 74453.

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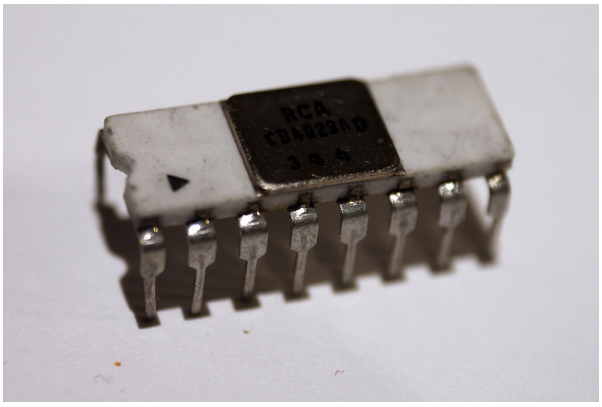
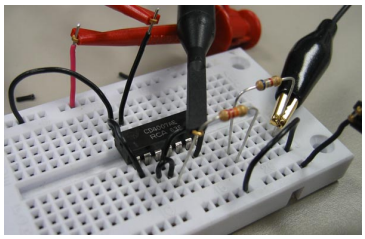
4000 series

This article is about integrated circuits. For other uses, see 4000 series (disambiguation).



A very early CD4029 counter IC, manufactured by RCA.

The **4000 series** is a family of industry-standard integrated circuits (IC) which implement a variety of logic functions using Complementary Metal–Oxide–Semiconductor (CMOS) technology, and are still in use today. They were introduced by RCA as *CD4000 COS/MOS* series in 1968, as a lower power and more versatile alternative to the 7400 series of transistor-transistor logic (TTL) logic chips.[1] Almost all IC manufacturers active during the era fabricated chips from this series. RCA sometimes advertised the line as COSMOS, standing for COmplementary Symmetry Metal-Oxide Semiconductor. The naming system followed the RCA convention of CA for analog, CD for digital, but did not relate to the Texas Instruments SN7400 series numbering scheme.


The CD4007 on a breadboard

4000 series parts have the advantage of lower power consumption, wider range of supply voltages (3 V to 15 V), and simpler circuit design due to the vastly increased fanout. However their slower speed (initially about 1 MHz operation, compared with bipolar TTL's 10 MHz) limits their applications to static or slow speed designs. New fabrication technology has largely overcome the speed problems, while retaining backward compatibility with most circuit designs. Although all semiconductors can be damaged by electrostatic discharge, the high impedance of CMOS inputs makes them more susceptible than bipolar transistor-based, TTL, devices. Eventually, the advantages of CMOS (especially the later series such as 74HC) edged out the older TTL chips, but at the same time ever increasing LSI techniques edged out the modular chip approach to design. The 4000 series is still widely available, but perhaps less important than it was two decades ago.

The series was extended in the late 1970s and 1980s to include new types which implemented new functions, or were better versions of existing chips in the 4000 series. Most of these newer chips were given 45xx and 45xxx designations, but are usually still regarded by engineers as part of the 4000 series.

In the 1990s, some manufacturers (e.g. Texas Instruments) ported the 4000 series to their newer HCMOS technology with devices such as the 74HCT4060 providing equivalent functionality to a 4060 IC but with greater speed.

The 4000 series integrated circuits have been used in space satellites for many decades.[2][3]

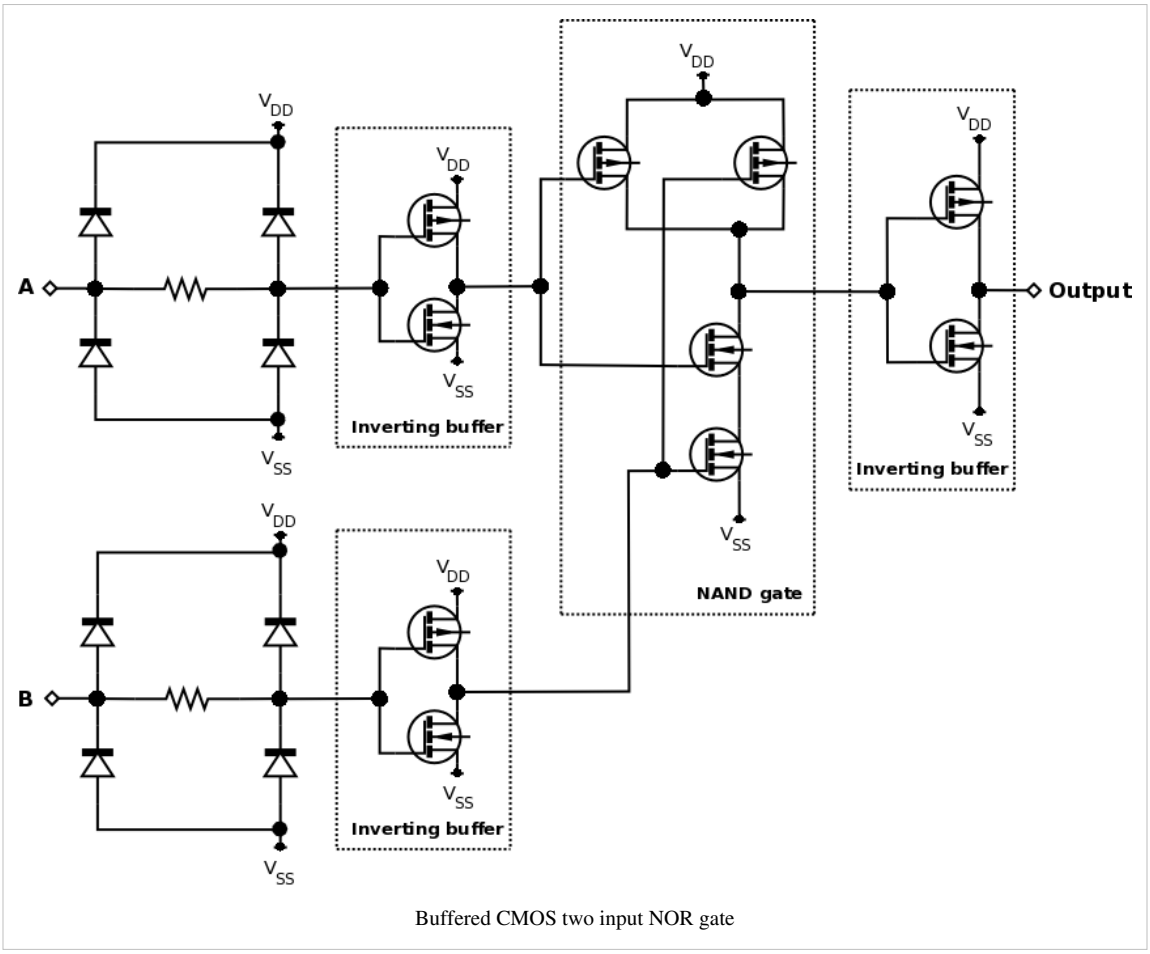
Design considerations

The original 4000 series was available in either unbuffered or buffered inputs and outputs. The buffered outputs can source or sink more current than the unbuffered outputs, eliminating the need for discrete switching transistors in some designs. The buffered versions also have faster output switching times, as the signal rise time of the buffered output stage is faster than that of an unbuffered device. However the overall propagation delay through the buffered versions is higher due to the additional circuitry.[4][5] The buffered devices are more susceptible to output oscillation with slow-changing inputs. Designers must evaluate the choice of buffered or unbuffered parts according to the nature of the circuit in which the devices are being used. The additional input and output gates on the buffered parts

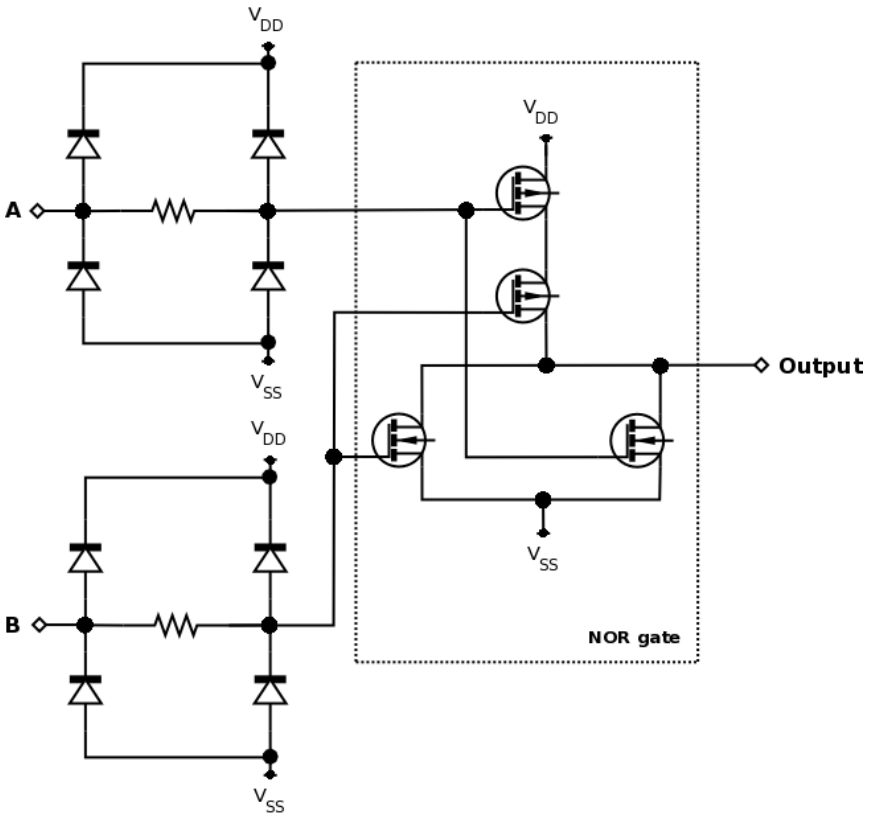
also make them marginally less susceptible to damage by electrostatic discharge (ESD).

Although the original designation for unbuffered and buffered parts was the addition of an 'A' or 'B' suffix to the part code (e.g.: 4000A = unbuffered, 4000B = buffered), some manufacturers (e.g.: Texas Instruments) later changed to using UB (unbuffered) and B (buffered) suffixes (e.g.: 4000UB and 4000B).

The diagrams below show the construction differences between a simple buffered and unbuffered CMOS NOR logic gate. Note that the logic gate at the core of the buffered part is actually a NAND gate, but the overall function of the complete circuit is a NOR gate due to the logic inversions performed by the buffers. (A negated NAND with negated inputs becomes a NOR as defined by De Morgan's laws in Boolean Algebra.) The clamping diodes on the inputs are to offer some protection against ESD.



Buffered CMOS two input NOR gate



Unbuffered CMOS two input NOR gate

The 4000 series permits the use of "cookbook" design, where standard circuit elements can be created, shared, and connected to other circuits with few, if any, connection difficulties. This greatly speeds the design of new hardware by reusing standard approaches to circuit design. In contrast, TTL circuits, while similarly modular, often require much more careful interfacing, since the limited fanout (and fan-in) require that the loading of each output be carefully considered. (Some later TTL families, like 74LS reduce this problem with fanouts of 20.) It is also much easier to prototype LSI designs using the 4000 series and get repeatable and transferable results when moving to the more integrated design.

Some care needs to be taken with the design of circuits using CMOS chips. Many parts offer multiple logic gates in a single package and it is common to not need all of them. An engineer who forgets to 'tie off' (connect the unused gate inputs to VSS or VDD) may find the chip draws excessive current. The problem is caused by biasing in each gate. With the inputs disconnected, the gates may be biased into a mode where the outputs are partially conducting; this leaves the output buffer drawing a great deal of current since it is not fully on or off, creating a low resistance current path between the power supply rails.

Example common 4000 series chips

Main article: List of 4000 series integrated circuits

- 4000 - Dual 3-Input NOR Gate and Inverter
- 4001 - Quad 2-Input NOR Gate
- 4002 - Dual 4-Input NOR Gate OR Gate
- 4008 - 4-Bit Full Adder
- 4010 - hex non-inverting buffer
- 4011 - Quad 2-Input NAND Gate
- 4017 - Decade Counter / Johnson Counter
- 4511 - BCD to 7-segment LED driver

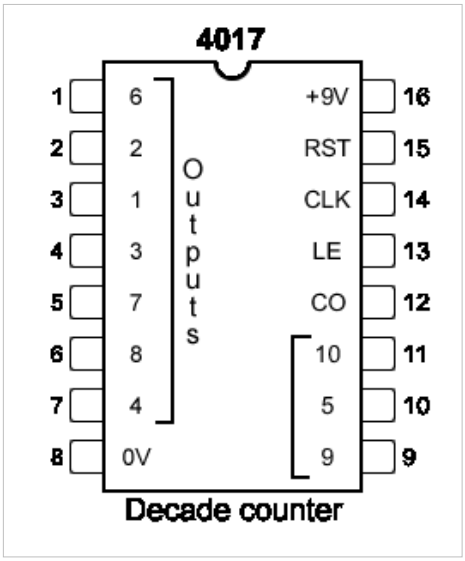
Notable parts

A few parts are notable in the 4000 series because of their level of integration compared to other chips. This list is intentionally incomplete and is meant to provide a sample of the more interesting parts in the series. Devices useful for switching analog signals (such as the 4066, and 4051 to 4053) have continued to enjoy popularity in some audio designs (although non-4000 series chips, often with less distortion, are now available).

4017 decade counter

The **4017 IC** is a 16-pin CMOS decade counter from the 4000 series. It takes clock pulses from the clock input, and makes one of the ten outputs come on in sequence each time a clock pulse arrives.

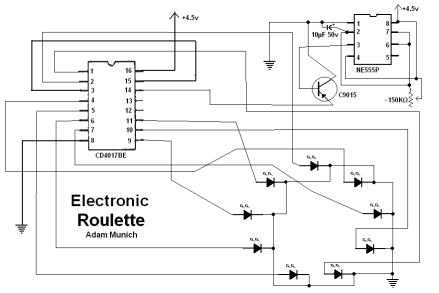
Pinout



Pin number	Name	Purpose
1	6	The 6th sequential output
2	2	The 2nd sequential output
3	1	The 1st sequential output
4	3	The 3rd sequential output
5	7	The 7th sequential output
6	8	The 8th sequential output
7	4	The 4th sequential output
8	0 V, V_{DD}	The connection to the 0 V rail
9	9	The 9th sequential output
10	5	The 5th sequential output
11	10	The 10th sequential output
12	CO	**C**arry **o**ut output - outputs high on counts 0 to 4, outputs low on counts 5 to 9 (thus a transition from low to high occurs when counting from 9 back to 0)
13	LE	**L**atch **e**nable - latches on the current output when high (i.e. the chip counts when LE is low)
14	CLK	**Cl**oc**k** in
15	RST	**Res**e**t** - sets output 1 high and outputs 2 through 10 low, when taken high
16	+9 V, V_{CC}	The connection to the $+V_{CC}$ rail (voltage between +3 V and +15 V)

Example: Electronic Roulette

The circuit diagram on the right shows how to create a game of roulette using the 4017 decade counter and various other electronic parts. The variable resistor adjusts the spin speed.

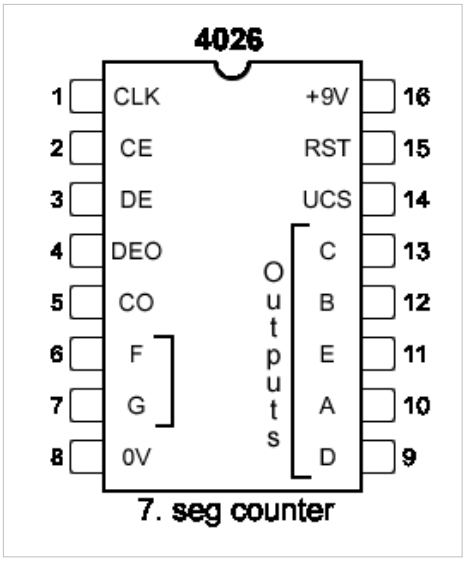


Electronic Roulette circuit diagram.

4026 counter and display decoder

The **4026 IC** is a 16-pin CMOS seven-segment counter from the 4000 series. It counts clock pulses and returns the output in a form which can be displayed on a seven-segment display. This avoids using a binary-coded decimal to seven-segment decoder, but it can only be used to display the (decimal) digits 0-9.

Pinout

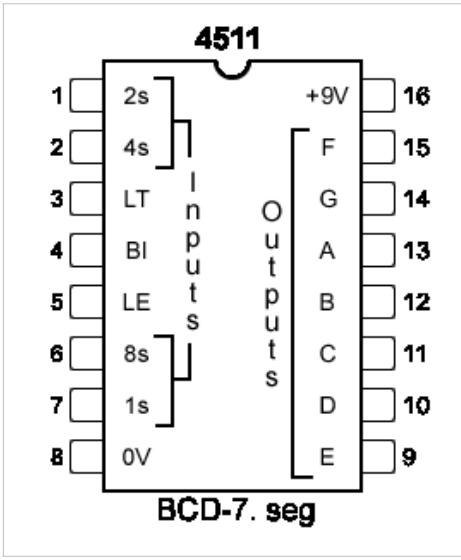


Pin number	Name	Purpose
1	CLK	**C**lo**ck** in
2	CI	**C**lock **i**nhibit - when low, clock pulses increment the seven-segment
3	DE	**D**isplay **e**nable - the chip outputs to the seven-segment when this is high (i.e. when it is low, the seven-segment is off) - useful to conserve battery life, for instance
4	DEO	**D**isplay **e**nable **o**ut - for chaining 4026s
5	CO	**C**arry **o**ut output - Is high when changing from 9 to 0. It provides an output at 1/10 of the clock frequency, to drive the clock input of another 4026 to provide multi-digit counting.
6	F	Output for the seven-segment's **F** input
7	G	Output for the seven-segment's **G** input
8	V_{DD}	The connection to the 0 V rail
9	D	Output for the seven-segment's **D** input
10	A	Output for the seven-segment's **A** input
11	E	Output for the seven-segment's **E** input
12	B	Output for the seven-segment's **B** input
13	C	Output for the seven-segment's **C** input
14	UCS	**U**ngated **C**-segment - an output for the seven-segment's **C** input which is not affected by the **DE** input. This output is high unless the count is 2, when it goes low.
15	RST	**Reset** - resets all outputs to low when taken high
16	V_{SS}	The connection to the +9 V rail

4511 BCD to seven-segment decoder

The **4511 IC** is a 16-pin CMOS BCD to seven-segment decoder from the 4000 series. It takes the binary-coded decimal from a binary counter and decodes it to drive a common cathode seven-segment display.

Pinout



Pin number	Name	Purpose
1	2s	Input for the 2s bit from the binary counter
2	4s	Input for the 4s bit from the binary counter
3	LT	**L**amp **t**est - when low, the chip takes all the segments on the display high (to test connections, etc.)
4	BI	**B**lanking **i**nput - when low, the chip does not output to the display - to conserve battery life, for instance
5	LE	**L**atch **e**nable - latches on the current output when high (i.e. the inputs change the output when LE is low)
6	8s	Input for the 8s bit from the binary counter
7	1s	Input for the 1s bit from the binary counter
8	0 V, V_{DD}	The connection to the 0 V rail
9	E	Output for the seven-segment's **E** input
10	D	Output for the seven-segment's **D** input
11	C	Output for the seven-segment's **C** input
12	B	Output for the seven-segment's **B** input
13	A	Output for the seven-segment's **A** input
14	G	Output for the seven-segment's **G** input
15	F	Output for the seven-segment's **F** input
16	+9 V, V_{CC}	The connection to the +9 V rail

References

[1] Wright, Maury. *Milestones That Mattered: CMOS pioneer developed a precursor to the processor* EDN, 6/22/2006 (http://www.edn.com/article/CA6343247.html)
[2] "Attitude control magnetometer" (http://magnetometer.com/wp-content/uploads/attitude-control-magnetometer.pdf)
[3] "AO-40 RUDAK Experiment Controller" (http://www.gag.com/~bdale/talks/2002/think/amsat/Sources/smallsat.pdf)
[4] Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics. Texas Instruments (http://focus.ti.com/lit/an/scha004/scha004.pdf)
[5] Lancaster, Don. *CMOS Cookbook*, ISBN 0-672-21398-2

External links

- List of 4000 series ICs (http://www.standardics.nxp.com/products/hef/all/) manufactured by NXP Semiconductors
- Thorough list of 4000 series ICs (http://www.kpsec.freeuk.com/components/cmos.htm)
- 4000B Series CMOS Functional Diagrams (http://www.samengstrom.com/nxl/7901/cmos_functional_diagram_page.en.html)
- 4000 Series Logic and Analog Circuitry, By James M Bryant (http://www.analog.com/static/imported-files/rarely_asked_questions/4000_Series_Article.pdf)

List of 4000 series integrated circuits

List of the CMOS 4000 series

- 4000 series - Family specification [1] - The family specification applies to each of the following circuits.
- 4000 [2] - Dual 3-input NOR gate + 1 NOT gate
- 4001 [2] - Quad 2-input NOR gate
- 4002 [2] - Dual 4-input NOR gate
- 4006 [3] - 18-stage shift register
- 4007 [4] - Dual complementary pair + 1 NOT gate
- 4008 [5] - 4-bit binary full adder
- 4009 [6] - Hex inverting buffer (replaced by 4049)
- 4010 [6] - Hex non-inverting buffer (replaced by 4050)
- 4011 [7] - Quad 2-Input NAND gate
- 4012 [7] - Dual 4-input NAND gate
- 4013 [8] - Dual D-type flip-flop
- 4014 [9] - 8-stage shift register
- 4015 [10] - Dual 4-stage shift register
- 4016 [11] - Quad bilateral switch
- 4017 [12] - Decade counter with 10 decoded outputs (5-stage Johnson counter)
- 4018 [13] - Presettable divide-by-N counter
- 4019 [14] - Quad AND/OR Select Gate
- 4020 [15] - 14-stage binary ripple counter
- 4021 [16] - 8-stage shift register
- 4022 [12] - Octal counter with 8 decoded outputs (4-stage Johnson counter)
- 4023 [17] - Triple 3-input NAND gate
- 4024 [15] - 7-Stage Binary Ripple Counter
- 4025 [2] - Triple 3-input NOR gate
- 4026 [18] - Decade counter with decoded 7-segment display outputs and display enable

- 4027 [19] - Dual J-K master-slave flip-flop
- 4028 [20] - BCD to decimal (1-of-10) decoder
- 4029 [21] - Presettable up/down counter, binary or BCD-decade
- 4030 [22] - Quad XOR gate (replaced by 4070)
- 4031 [23] - 64-stage shift register
- 4032 [24] - Triple serial adder
- 4033 [18] - Decade counter with decoded 7-segment display outputs and ripple blanking
- 4034 [25] - 8-stage bidirectional parallel/serial input/output register
- 4035 [26] - 4-stage parallel-in/parallel-out (PIPO) shift register
- 4038 [24] - Triple serial adder
- 4040 [15] - 12-stage binary ripple counter
- 4041 [27] - Quad true/complement buffer
- 4042 [28] - Quad D-type latch
- 4043 [29] - Quad NOR R/S latch with tristate outputs
- 4044 [29] - Quad NAND R/S latch with tristate outputs
- 4045 [30] - 21-stage counter
- 4046 [31] - Phase-locked loop with VCO
- 4047 [32] - Monostable/astable multivibrator
- 4048 [33] - Multifunctional expandable 8-input gate with tristate output
- 4049 [34] - Hex inverter
- 4050 [34] - Hex buffer/converter (non-inverting)
- 4051 [35] - 8-channel analog multiplexer/demultiplexer
- 4052 [35] - Dual 4-channel analog multiplexer/demultiplexer
- 4053 [35] - Triple 2-channel analog multiplexer/demultiplexer
- 4054 [36] - 4-segment LCD driver
- 4055 [36] - BCD to 7-segment decoder/LCD driver with "display-frequency" output
- 4056 [36] - BCD to 7-segment decoder/LCD driver with strobed-latch function
- 4059 [37] - Programmable divide-by-N counter
- 4060 [38] - 14-stage binary ripple counter and oscillator
- 4062 - Logic dual 3 majority gate
- 4063 [39] - 4-bit Digital comparator
- 4066 [40] - Quad Analog switch (Low "ON" Resistance)
- 4067 [41] - 16-channel analogue multiplexer/demultiplexer (1-of-16 switch)
- 4068 [42] - 8-input NAND gate
- 4069 [43] - Hex NOT gate (Inverter)
- 4070 [44] - Quad XOR gate
- 4071 [45] - Quad 2-input OR gate
- 4072 [46] - Dual 4-input OR gate
- 4073 [47] - Triple 3-input AND gate
- 4075 [46] - Triple 3-input OR gate
- 4076 [48] - Quad D-type register with tristate outputs
- 4077 [44] - Quad 2-input XNOR gate
- 4078 [49] - 8-input NOR gate
- 4081 [50] - Quad 2-input AND gate
- 4082 [51] - Dual 4-input AND gate
- 4085 [51] - Dual 2-wide, 2-input AND/OR invert (AOI)
- 4086 [52] - Expandable 4-wide, 2-input AND/OR invert (AOI)

- 4089 [53] - Binary rate multiplier
- 4093 [54] - Quad 2-input Schmitt trigger NAND gate
- 4094 [55] - 8-stage shift-and-store bus
- 4095 [56] - Gated "J-K" (non-inverting)
- 4096 [56] - Gated "J-K" (inverting and non-inverting)
- 4097 [41] - Differential 8-channel analog multiplexer/demultiplexer
- 4098 [57] - Dual one-shot monostable
- 4099 [58] - 8-bit addressable latch
- 4104 [59] - Quad Low-to-High Voltage Translator with tristate outputs
- 4106 - Hex Schmitt Trigger
- 4160 - Decade counter with asynchronous clear
- 4161 - 4-bit Binary counter with asynchronous clear
- 4162 - Decade counter with synchronous clear
- 4163 - 4-bit Binary counter with synchronous clear
- 4175 - Quadruple D-Type Flip Flop
- 4192 - Presettable Up-Down Counter
- 4500 - Industrial Control Unit (ICU)
- 4502 [60] - Hex inverting buffer (tristate)
- 4503 [61] - Hex non-inverting buffer with tristate outputs
- 4504 [62] - Hex voltage level shifter for TTL-to-CMOS or CMOS-to-CMOS operation
- 4505 - 64-bit, 1-bit per word Random Access Memory (RAM)
- 4508 [63] - Dual 4-bit latch with tristate outputs
- 4510 [64] - Presettable 4-bit BCD up/down counter
- 4511 [65] - BCD to 7-segment latch/decoder/driver
- 4512 [66] - 8-input multiplexer (data selector) with tristate output
- 4513 - BCD to 7-segment latch/decoder/driver (4511 plus ripple blanking)
- 4514 [67] - 1-of-16 decoder/demultiplexer active HIGH output
- 4515 [67] - 1-of-16 decoder/demultiplexer active LOW output
- 4516 - Presettable 4-bit binary up/down counter
- 4517 - Dual 64-stage shift register
- 4518 [68] - Dual BCD up counter
- 4519 [69] - Quad 2-input multiplexer (data selector)
- 4520 [70] - Dual 4-bit binary up counter
- 4521 - 24-stage frequency divider
- 4522 - Programmable BCD divide-by-N counter
- 4526 - Programmable 4-bit binary down counter
- 4527 [71] - BCD rate multiplier
- 4528 [72] - Dual Retriggerable Monostable Multivibrator with Reset
- 4529 - Dual 4-channel analog
- 4530 - Dual 5-input Majority Logical Gate
- 4531 - 12-bit Parity Tree
- 4532 [73] - 8-bit priority encoder
- 4536 [74] - Programmable Timer
- 4538 [75] - Dual Retriggerable Precision Monostable Multivibrator
- 4539 [76] - Dual 4-input multiplexer
- 4541 [77] - Programmable Timer
- 4543 [78] - BCD to 7-Segment Latch/Decoder/Driver with Phase Input

- 4551 - quad 2-channel analog Multiplexer/Demultiplexer
- 4553 [79] - 3-digit BCD counter
- 4555 [80] - Dual 1-of-4 decoder/demultiplexer active HIGH output
- 4556 [81] - Dual 1-of-4 decoder/demultiplexer active LOW output
- 4557 [82] - 1-to-64 Bit Variable Length Shift Register
- 4558 - BCD to 7-segment decoder (Enable, RBI and provides active–high output)
- 4560 [83] - NBCD adder
- 4562 - 128–bit Static Shift Register
- 4566 [84] - Industrial time-base generator
- 4569 - Programmable Divide-By-N, Dual 4-Bit Binary/BCD Down Counter
- 4572 [85] - Hex gate : quad NOT, single NAND, single NOR
- 4583 - Dual Schmitt Trigger
- 4584 [86] - Hex inverting schmitt trigger
- 4585 [87] - 4-bit Digital comparator
- 4724 - 8-bit addressable latch
- 4750 [88] - Frequency synthesizer
- 4751 - Universal divider
- 4794 - 8-Stage Shift-and-Store Register LED Driver
- 4894 - 12-Stage Shift-and-Store Register LED Driver
- 4938 - Dual Retriggerable Precision Monostable Multivibrator with Reset
- 4952 - 8-channel analog multiplexer/demultiplexer
- 40098 - 3-state hex inverting buffer
- 40100 [89] - 32-bit left/right Shift Register
- 40101 - 9-bit Parity Generator/Checker
- 40102 - Presettable 2-decade BCD down counter
- 40103 - Presettable 8-bit binary down counter
- 40104 - 4 bit bidirectional Parallel-in/Parallel-out PIPO Shift Register (tristate)
- 40105 [90] - 4-bit x 16 word FIFO Register
- 40106 [91] - Hex Inverting Schmitt-Trigger-(NOT gates)
- 40107 - dual 2-input NAND buffer/driver
- 40108 - 4x4-bit (tristate) synchronous triple-port register file
- 40109 [92] - Quad level shifter
- 40110 - Up/Down Counter-Latch-Decoder-Driver
- 40116 - 8-bit bidirectional CMOS-to-TTL level converter
- 40117 - Programmable dual 4-bit terminator
- 40147 [93] - 10-line to 4-line (BCD) priority encoder
- 40160 - Decade counter/asynchronous clear
- 40161 - Binary counter/asynchronous clear
- 40162 - 4-bit synchronous decade counter with load, reset, and ripple carry output
- 40163 - 4-bit synchronous binary counter with load, reset, and ripple carry output
- 40174 - Hex D-type flip-flop
- 40175 - Quad D-type flip-flop
- 40181 - 4-bit 16-functions arithmetic logic unit (ALU)
- 40192 [94] - Presettable 4-bit up/down BCD counter
- 40193 [94] - Presettable 4-bit up/down Binary counter
- 40194 [95] - 4-bit bidirectional universal shift register
- 40195 - 4-bit universal shift register

- 40208 - 4 x 4-bit (tristate) Synchronous triple-port register file
- 40240 - Buffer/Line driver; Inverting (tristate)
- 40244 - Buffer/Line Driver; Non-Inverting (tristate)
- 40245 - Octuple bus transceiver; (tristate) outputs,
- 40257 - Quad 2-line to 1-line Data Selector/Multiplexer (tristate)
- 40373 [96] - Octal D-Type Transparent latch (tristate)
- 40374 [97] - Octal D-type flip-flop; positive-edge trigger (tristate)
- 45106 - Frequency synthesizer

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[2] http://www.datasheetcatalog.org/datasheets/150/108513_DS.pdf
[3] http://www.datasheetcatalog.org/datasheet2/4/096cakxcerg86i8id610cu0xd4wy.pdf
[4] http://www.datasheetcatalog.org/datasheets/105/108563_DS.pdf
[5] http://www.datasheetcatalog.org/datasheets2/99/99178_1.pdf
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[7] http://www.datasheetcatalog.org/datasheets/208/108647_DS.pdf
[8] http://www.datasheetcatalog.org/datasheets/228/108664_DS.pdf
[9] http://www.datasheetcatalog.org/datasheets/70/108688_DS.pdf
[10] http://www.datasheetcatalog.org/datasheets/228/108692_DS.pdf
[11] http://www.datasheetcatalog.org/datasheets/270/108713_DS.pdf
[12] http://www.datasheetcatalog.org/datasheets/320/108737_DS.pdf
[13] http://www.datasheetcatalog.org/datasheets/270/108781_DS.pdf
[14] http://www.datasheetcatalog.org/datasheet2/4/08ihxuoo2axhzcyojf40it39txcy.pdf
[15] http://www.datasheetcatalog.org/datasheet2/9/0paqd91zcls9g4akywgtgso3y1ky.pdf
[16] http://www.datasheetcatalog.org/datasheets/90/108848_DS.pdf
[17] http://www.datasheetcatalog.org/datasheets/134/108885_DS.pdf
[18] http://www.datasheetcatalog.org/datasheet2/1/03gjao0ck9g0glqesyly2s563d7y.pdf
[19] http://www.datasheetcatalog.org/datasheet2/6/0rowk82e1wfe4yejr5itlgo1tcky.pdf
[20] http://www.datasheetcatalog.org/datasheet2/c/0hxr6urfrdjrdwt9wd8odzsaicky.pdf
[21] http://www.datasheetcatalog.org/datasheet2/2/05uej9xrraz7l6rc4likrej1tapy.pdf
[22] http://www.datasheetcatalog.org/datasheet2/a/0s3q1u9weefx7gl79f9ha1s3qayy.pdf
[23] http://www.datasheetcatalog.org/datasheet2/9/0pjrldxw2xz62r1z0aahd2a36p3y.pdf
[24] http://www.datasheetcatalog.org/datasheets/270/84982_DS.pdf
[25] http://www.datasheetcatalog.org/datasheet2/4/09p7285l04wpeep3fax6hojqhkcy.pdf
[26] http://www.datasheetcatalog.org/datasheet2/9/0og11wds0f9ogj7ffzs7ikl4otky.pdf
[27] http://www.datasheetcatalog.org/datasheet2/a/0s230ap3le6i5l3esx48eklfoccy.pdf
[28] http://www.datasheetcatalog.org/datasheet2/9/0oqf0076icwadgde9su7g9oihq3y.pdf
[29] http://www.datasheetcatalog.org/datasheet2/f/0xjord7w25gp833rh9d7l2sw1swy.pdf
[30] http://www.datasheetcatalog.org/datasheet2/0/01piqtrfrz55gdsgrdqx2gp44lky.pdf
[31] http://www.datasheetcatalog.org/datasheet2/6/0rs2lxolj6lew0llx95wkfal45yy.pdf
[32] http://www.datasheetcatalog.org/datasheet2/4/084klcd50i3au7uz078a46e95gyy.pdf
[33] http://www.datasheetcatalog.org/datasheet2/e/0lj0i18w98zpxra1z0659l7kehky.pdf
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