Understanding Embedded Software

RTOS [edit]

- Preemptive Scheduling (pdf)
- uCOS II tutorial (pdf)
- Critical Section (pdf)

Performance Optimization [edit]

- StarCore DSP tutorial (pdf)
- Computing Correlation Functions (pdf)

1. RTOS

(a) preemptive scheduling

George Mason U, CPU Scheduling,
https://cs.gmu.edu/~astavrou/courses/CS_571_F09/CS571_Lecture4_Scheduling.pdf
Basic Concepts, When to schedule, Preemptive vs Non-preemptive,
Dispatcher,

Princeton, Kai Li,
https://www.cs.princeton.edu/courses/archive/fall09/cos318/lectures/ThreadImplementation.pdf

(b) RTOS - uCOS

Vanderbilt, EE276,
http://eecs.vanderbilt.edu/Courses/ee276/Fall06_lectures/10%20RTOS%20basics.pdf
Task, TCB, Task States,
RTOS Tasks, Reentrant functions

Vanderbilt, EECE6354,
http://www.isis.vanderbilt.edu/sites/default/files/GettingStarted.ppt
Multitasking, RTK,

http://www.isis.vanderbilt.edu/sites/default/files/Tasks.pptx
Multitasking, Task, Task Creating & Initializing an Application,
OS Initialization, Task creation, Initial Task, Critical Sections,
Semaphores, Binary Semaphore, Counting Semaphore

(c) Critical Section

Uoc.gr
http://www.csd.uoc.gr/~hy586/material/lectures/cs586-Section2.pdf
Until Peterson's algorithm

UWisc, EECE6354,
http://pages.cs.wisc.edu/~remzi/OSTEP/threads-locks.pdf
Multitasking, RTK,

Uregina,
http://www2.cs.uregina.ca/~hamilton/courses/330/notes/synchro/node3.html

- Critical Section (pdf)

Try 1 – working examples

```
lock = false;

P0:
while (true) {
    while (lock) { ; }
```

```
P1:
while (true) {
```

Wait for th
of the lock
Set the lo

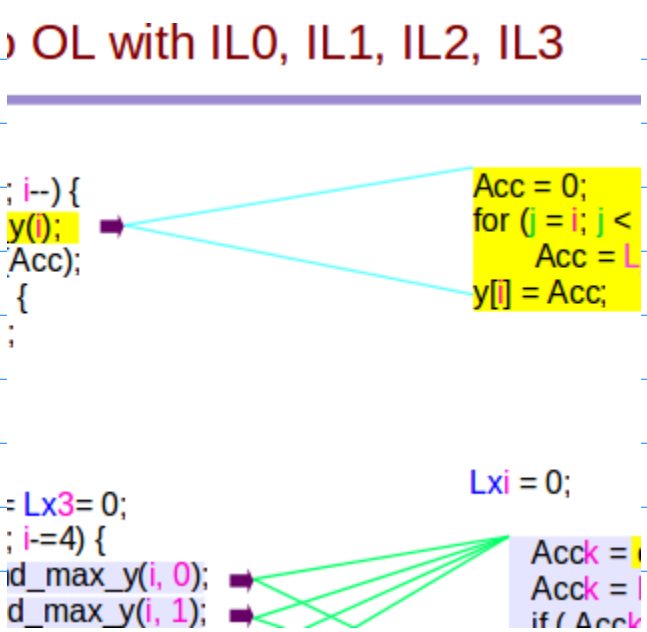
.

2. DSP Peformance Optimization Technique

- Computing Correlation Functions (pdf)

Based on

Cross Correlation
http://cache.freescale.com/files/dsp/doc/app_note/AN2266.pdf



3. ARM Assembly Programming

(a) Function Call / Stack / ATPCS ...

[PDF] Experiment 3 - Data Types, Data Structures and Functions
www.zap.org.au/elec2041-cdrom/unsw/elec2041/experiment3.pdf
Experiment 3: Data Types, Data Structures and Functions. This experiment further consolidates the programmer's view of computer architecture. It does this by ...

(b) Banked Registers / Operating Mode / System Calls / Interrupts ...

[PDF] Experiment 5 - Operating Modes, System Calls and Interrupts
www.cs.otago.ac.nz/cosc440/readings/arm-syscall.pdf
this experiment will only deal with the User, FIQ, IRQ and Supervisor modes of ... Bit 5 (the T bit) determines whether the processor runs in ARM state or in ...

(C) LDM, STM

IA, IB, DA, DB, FA, FD, EA, ED

[PDF] Lecture 7 Stacks and Subroutines Load/Store Multiple Instructions ...
www.ee.ic.ac.uk/pcheung/teaching/ee2_computing/Lecture_7.pdf
Nov 9, 2001 - Lecture 7 Stacks and Subroutines. ◇ LDR and STR instructions only load/store a single 32-bit word. ◇ ARM can load/store ANY subset of the ...

[PDF] 5. & 7. ARM: Architecture (3)(4) - Electrical and Computer Engineering
www.ece.cmu.edu/~ee349/lectures/05-07_arm_architecture_handout.pdf
5. & 7. ARM: Architecture (3)(4). Priya Narasimhan. Electrical & Computer Engineering. Carnegie Mellon University. h p://www.ece.cmu.edu/~ee349.