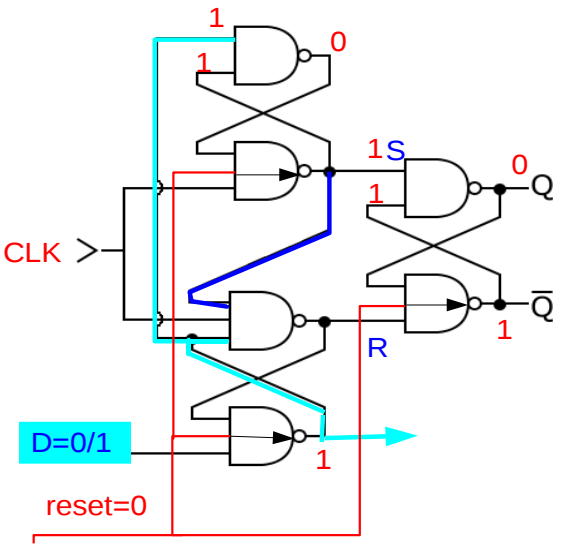


R	Clk	D	Q	Q'
0	X	X	0	1
1	r	0	0	1
1	r	1	1	0

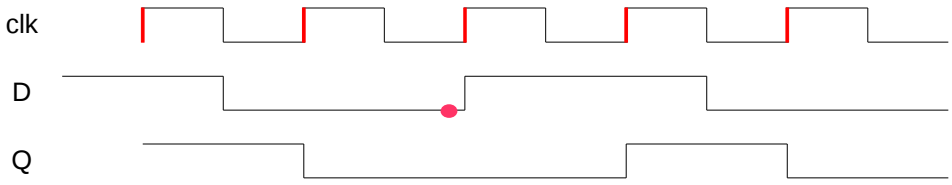
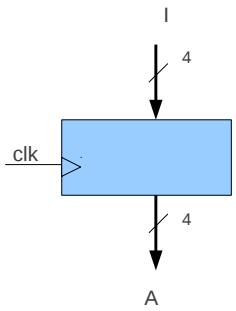
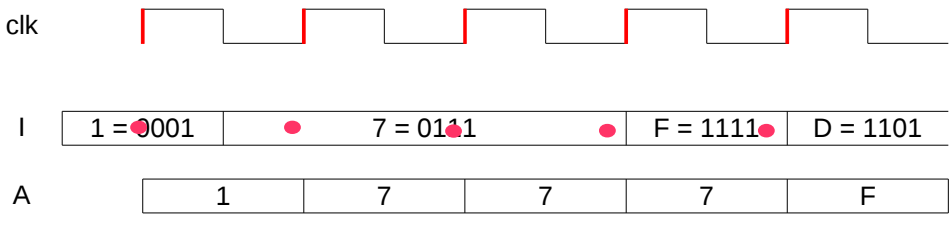


Fig 6.1





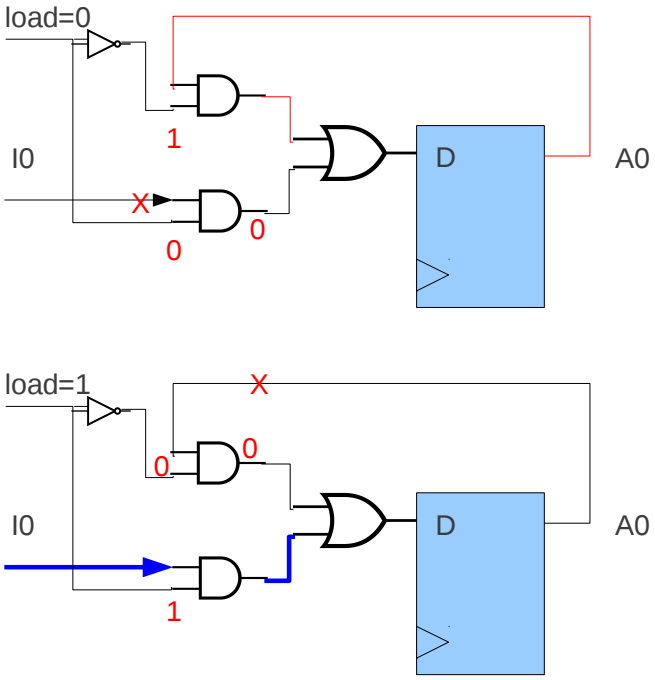
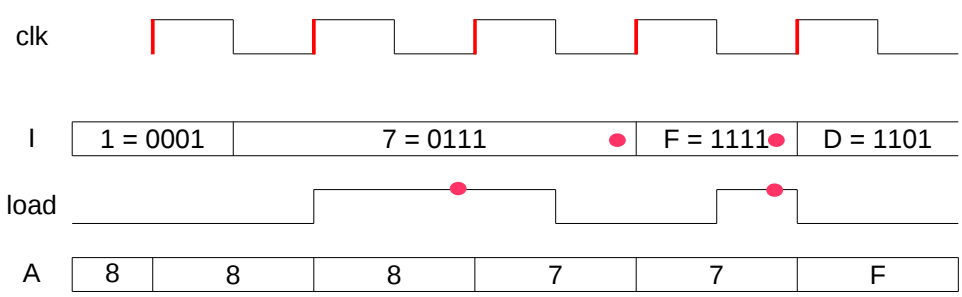
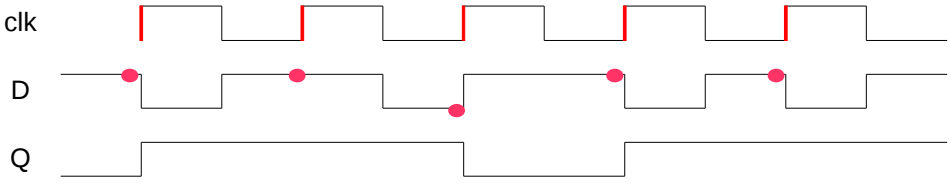
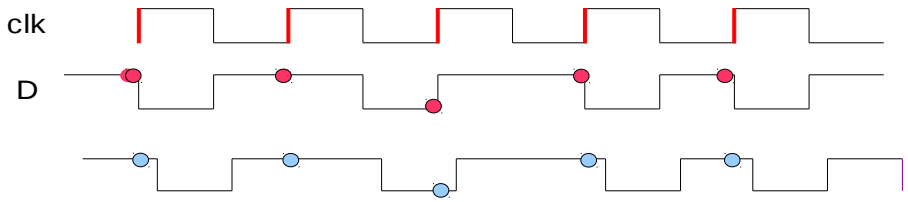
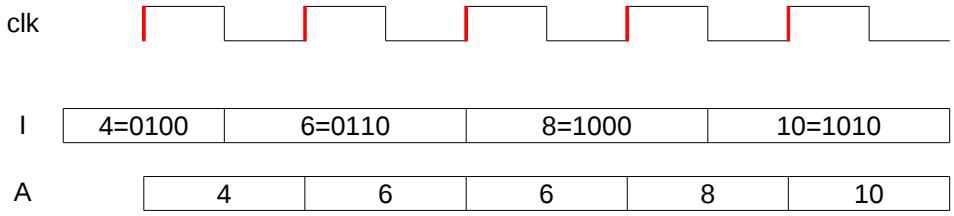


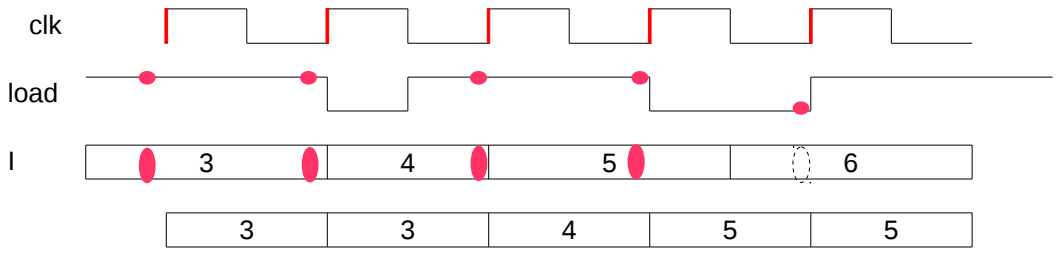
Fig 6.2 4-bit register with parallel load

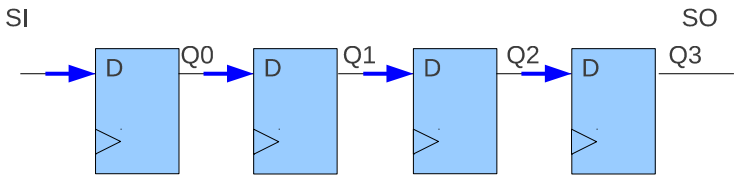


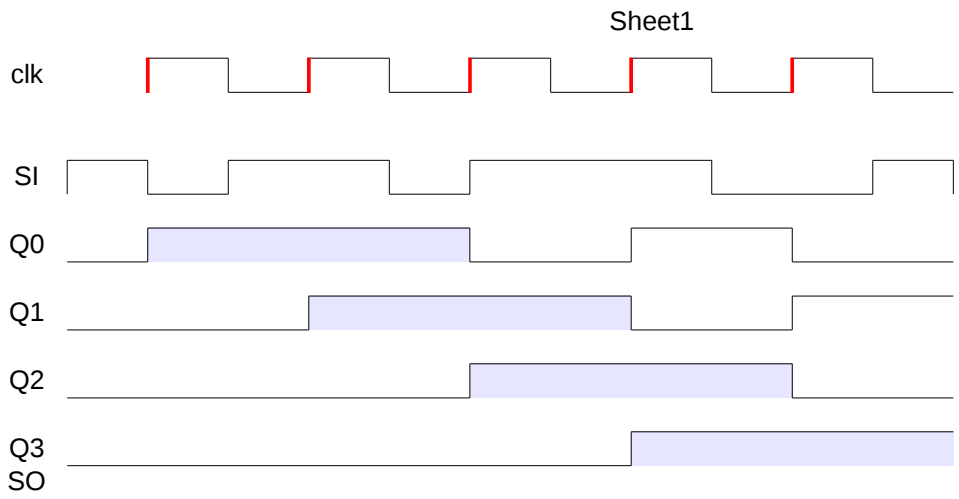


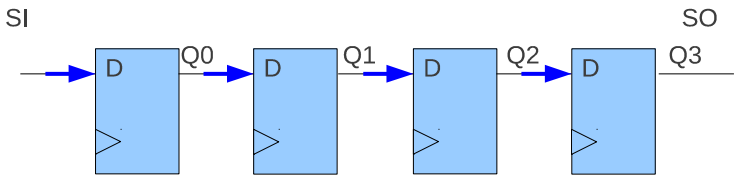

clk
D


clk
I
4=0100
6=0110
8=1000
10=1010
A
4
6
6
8
10


clk
load
I
3
4
5
6
3
3
4
5
5


SI
SO
D
Q0
D
Q1
D
Q2
D
Q3


Sheet1
clk
SI
Q0
Q1
Q2
Q3
SO


SI
SO
D
Q0
D
Q1
D
Q2
D
Q3

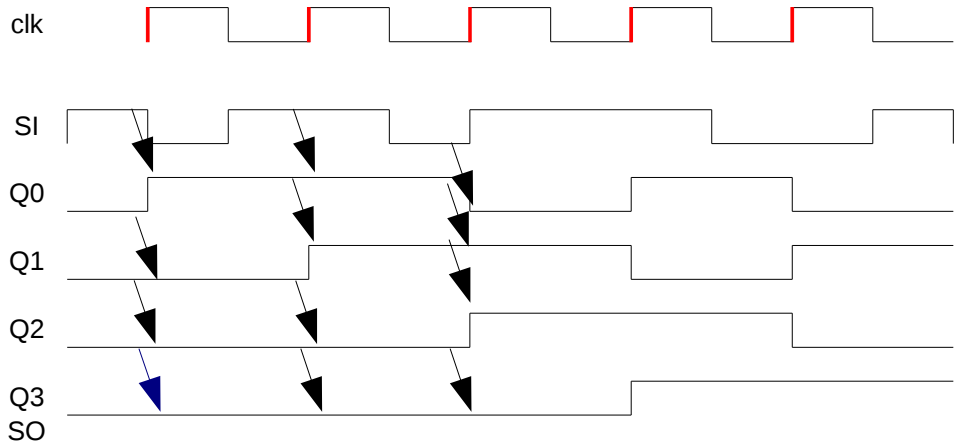
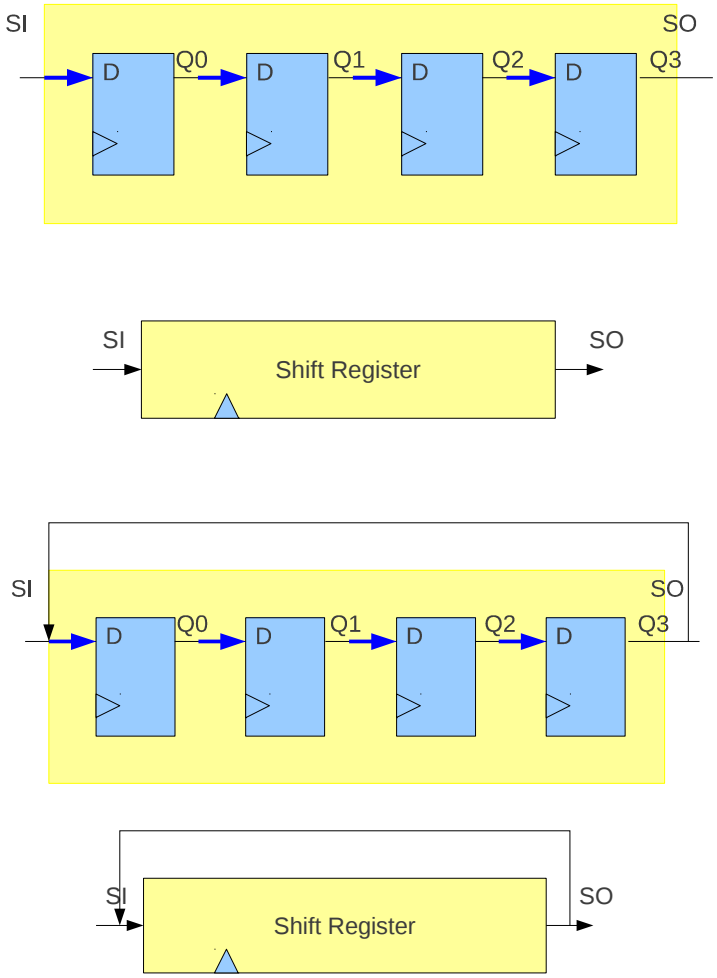
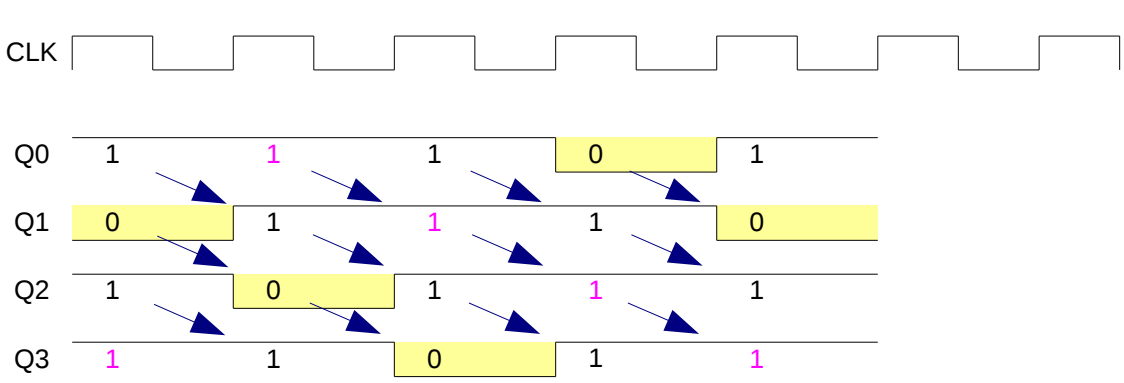
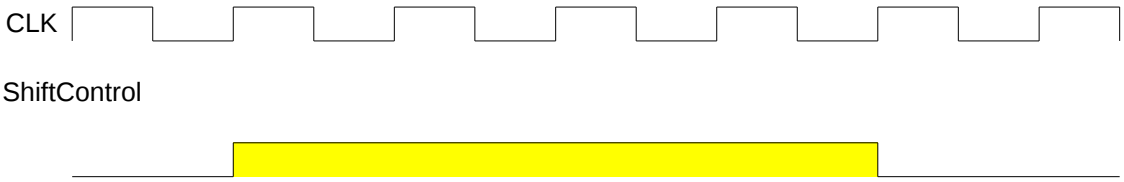

clk
SI
Q0
Q1
Q2
Q3
SO

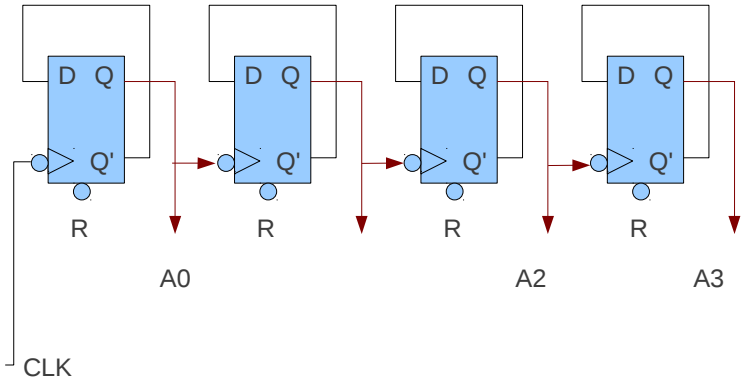
Fig 6.4

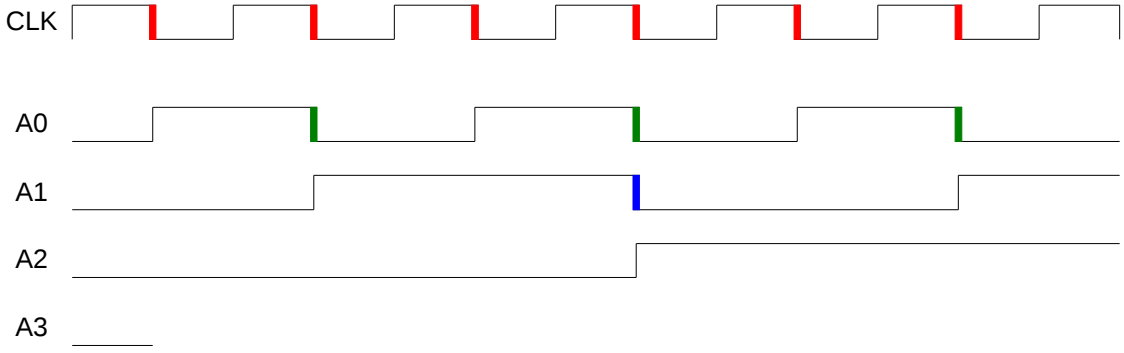





CLK
ShiftControl


CLK.ShiftControl


D Q
Q'
R
D Q
Q'
R
D Q
Q'
R
D Q
Q'
R
A0
A2
A3
CLK


CLK
A0
A1
A2
A3