

MetaStable State (3E)

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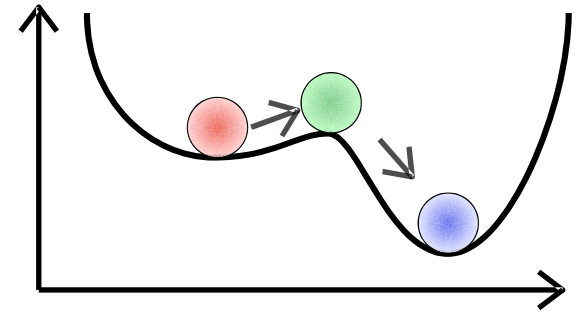
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Meta

Meta (from the Greek preposition μετά = "after", "beyond", "adjacent", "self", also commonly used in the form μετα- as a prefix in Greek, with variants μετ- before vowels and μεθ- "meth-" before aspirated vowels), is a prefix used in English (and other Greek-owing languages) to indicate a concept which is an abstraction from another concept, used to complete or add to the latter.

For example, metadata are data about data (who has produced them, when, what format the data are in and so on).

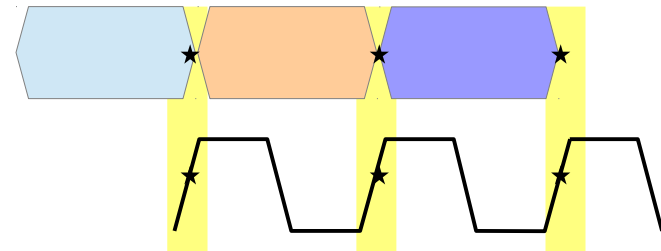
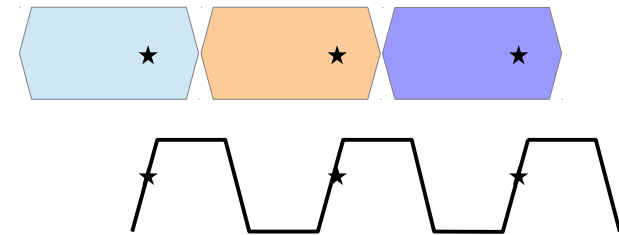
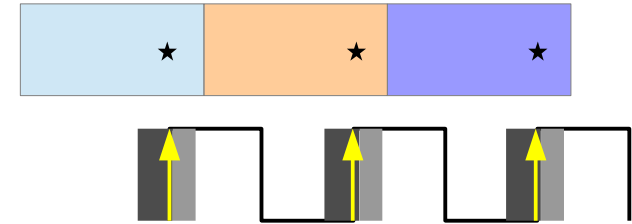


Metastability

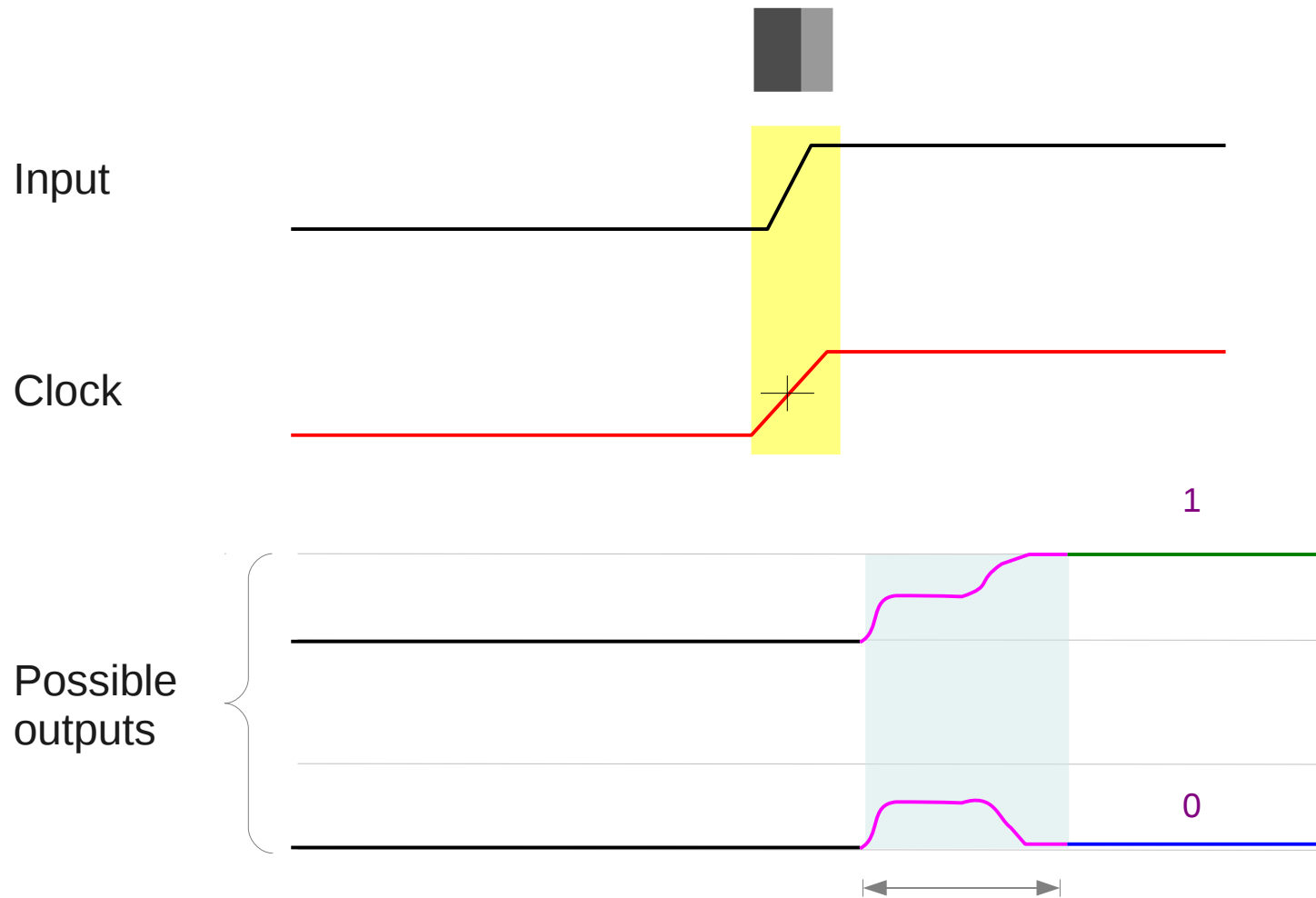
Metastability in electronics is the ability of a digital electronic system **to persist for an unbounded time** in an **unstable equilibrium** or **metastable state**.

In **metastable states**, the circuit may be **unable to settle** into a stable '0' or '1' logic level **within the time** required for proper circuit operation.

As a result, the circuit can act in **unpredictable ways**, and may lead to a system failure, sometimes referred to as a "glitch".



Possible Metastable Outputs

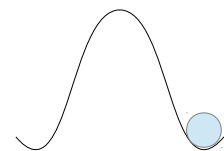
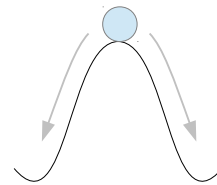
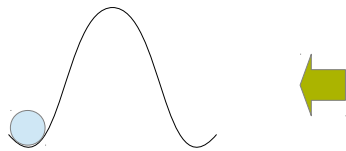
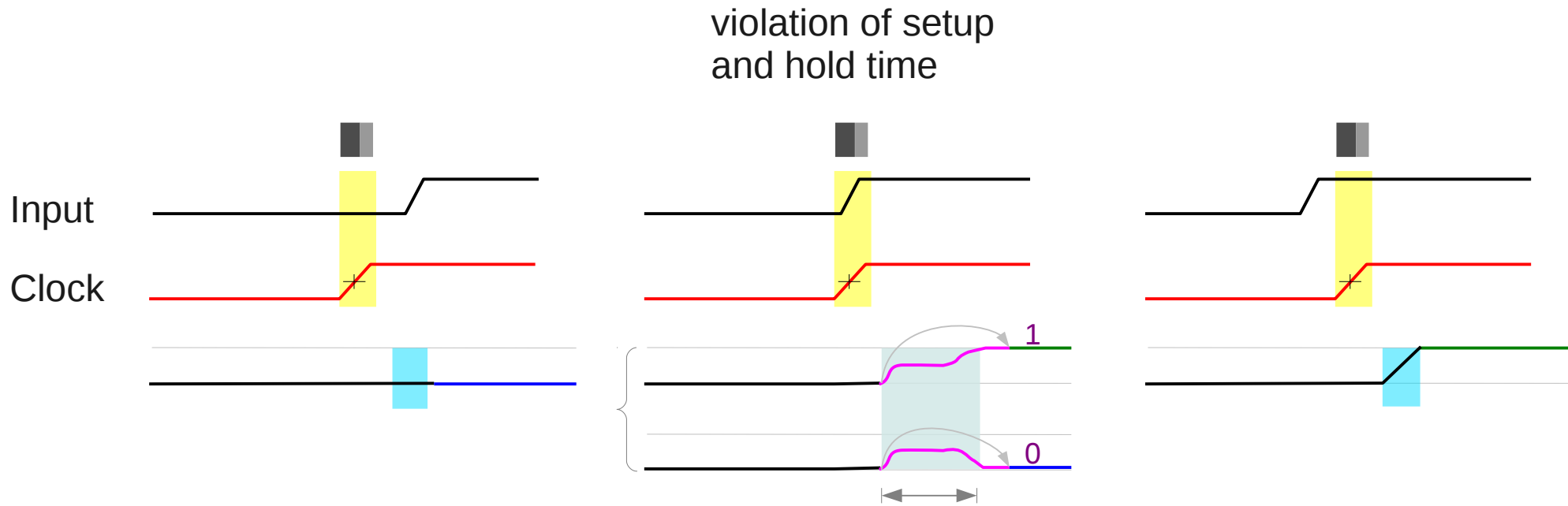


Metastable State (3C)

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Young Won Lim
10/30/13

Metastability

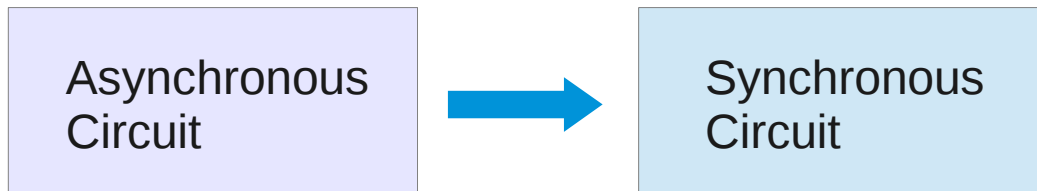


Setup Time and Hold Time Constraints

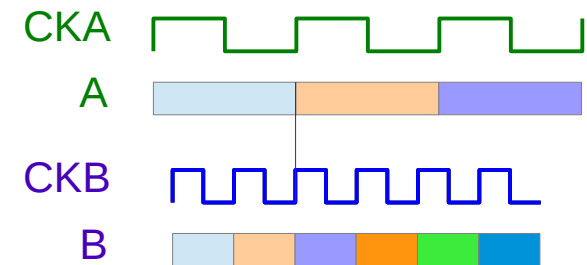
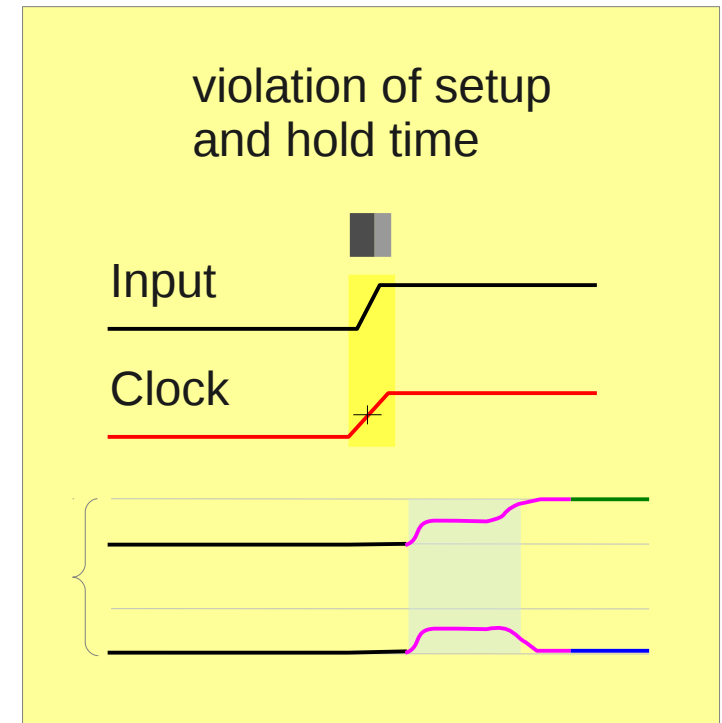
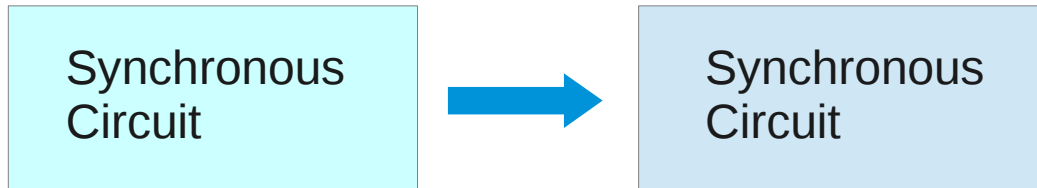
Input

Clock

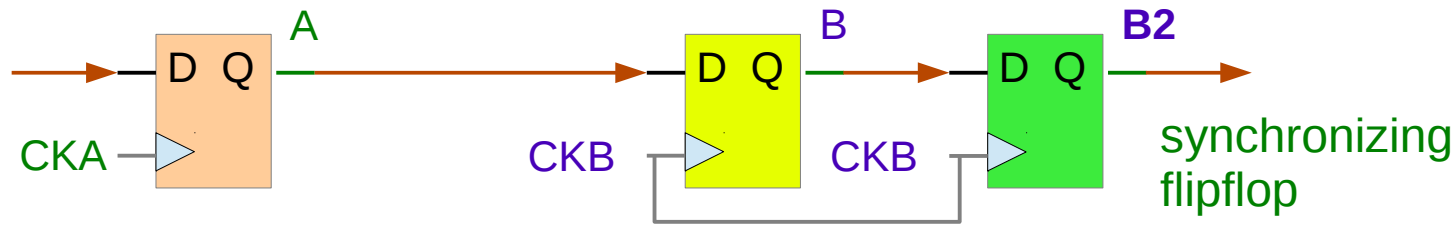
Causes of Metastability



Push button



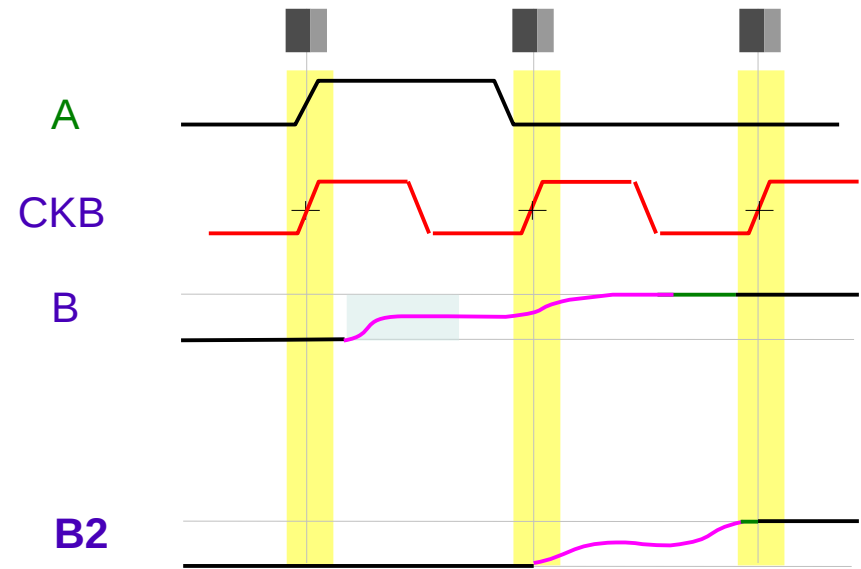
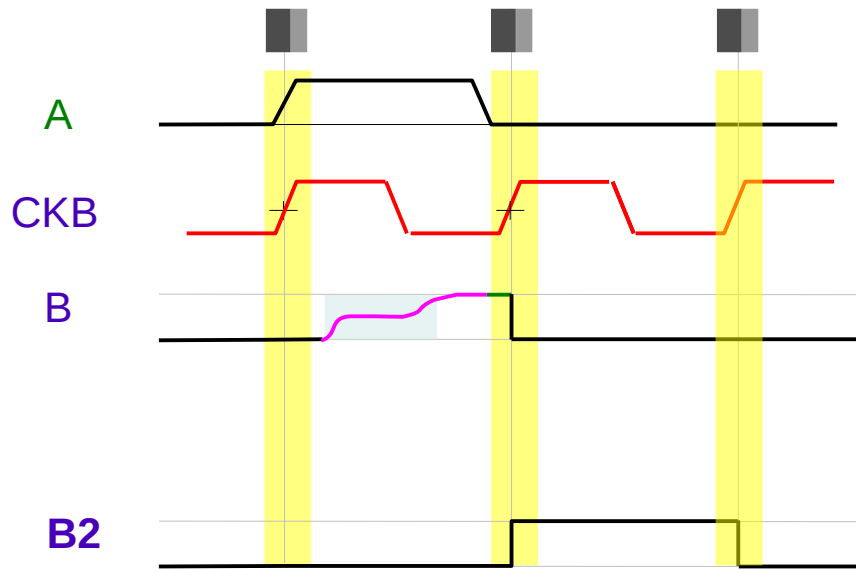
Synchronizing FlipFlops



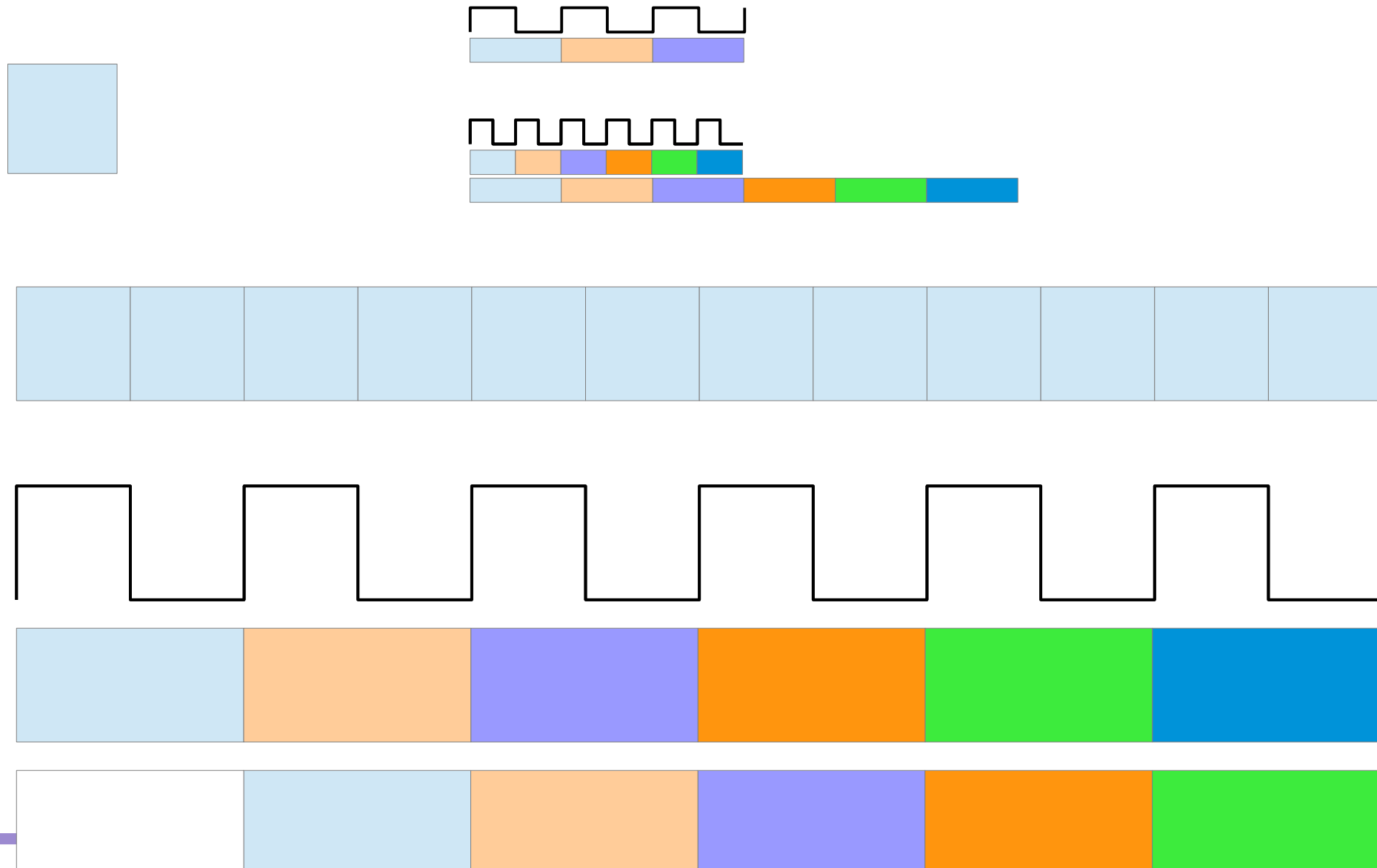
The likelihood of the synchronizing flipflop is **less** than that of the first flipflop going metastable.

Usually the metastable period is not so long compared to the clock period but the following case can happen

The probability never goes to zero



NOR-based SR Latch



Metastable State (3C)

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References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
- [3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.