

# SR Latch Forbidden State (3C)

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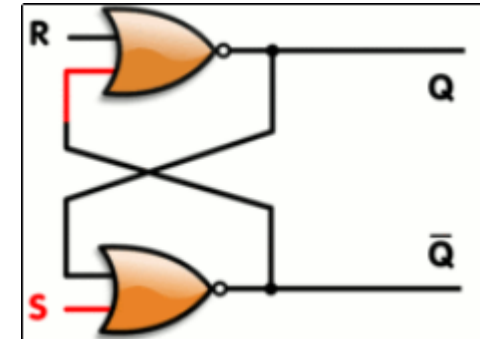
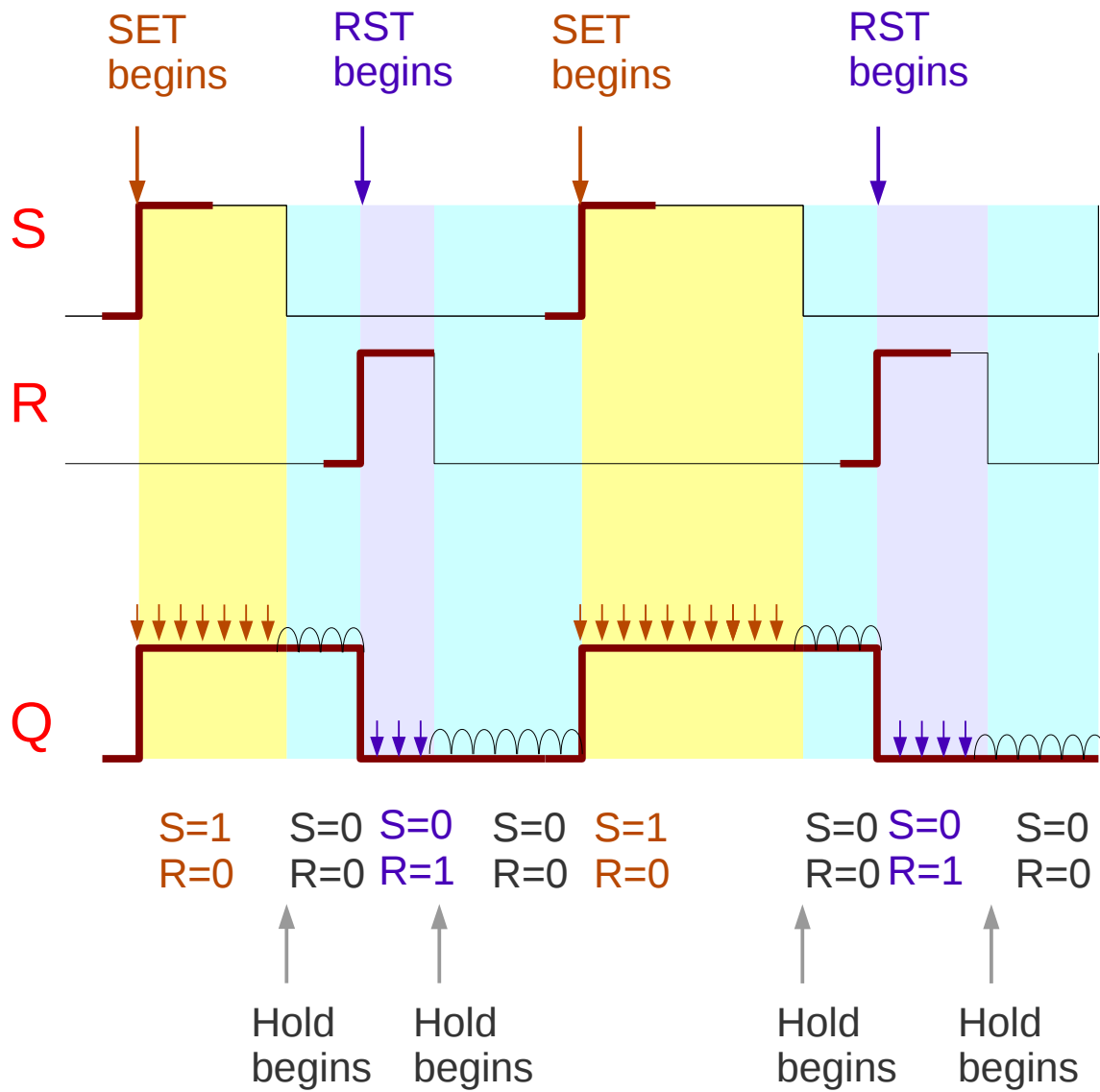
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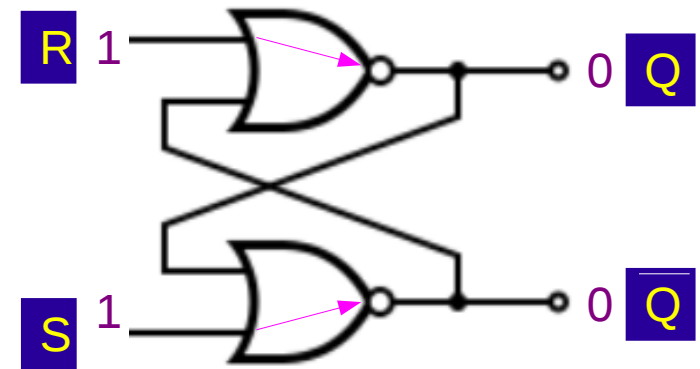
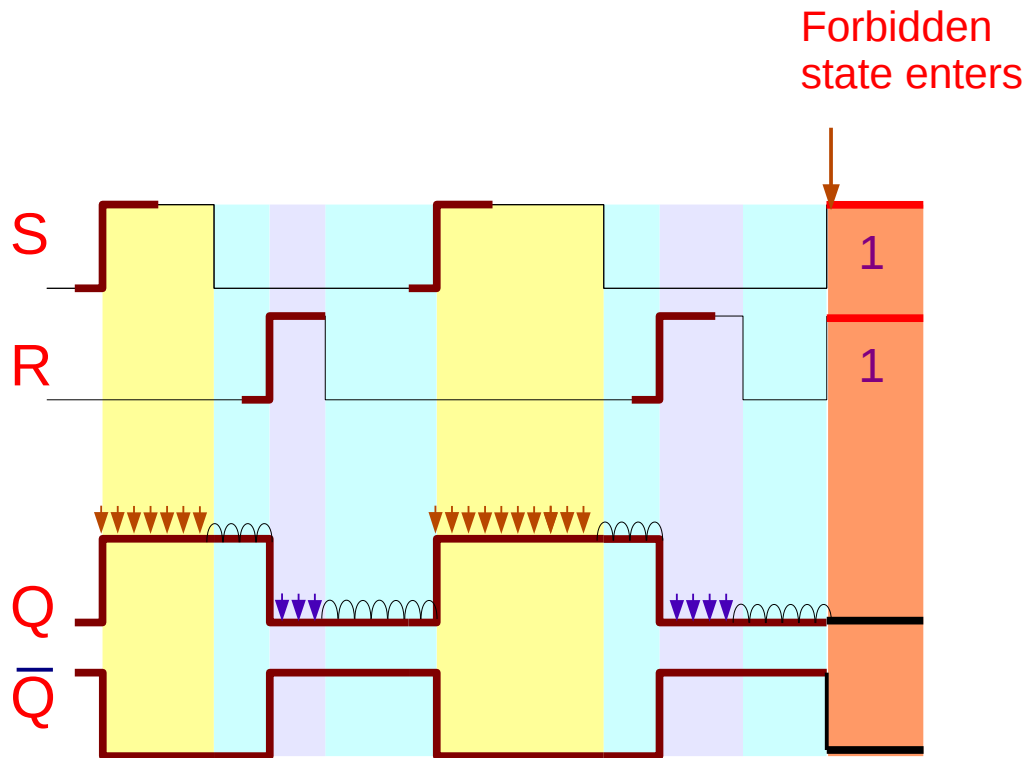
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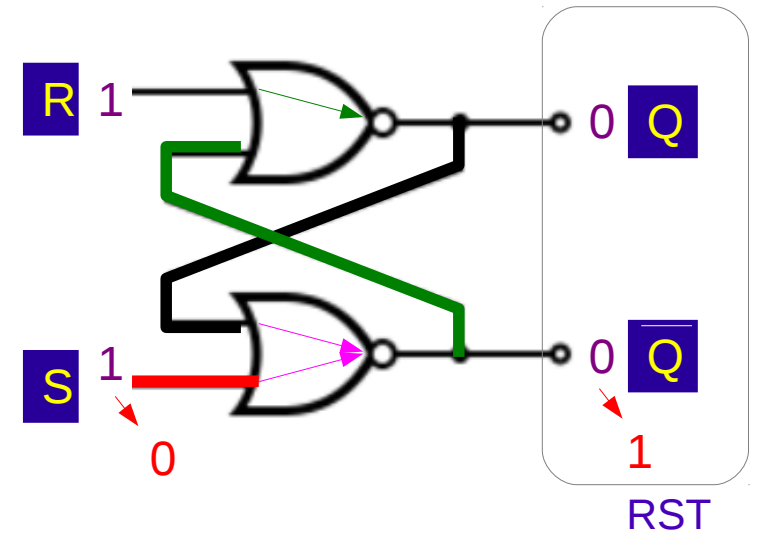
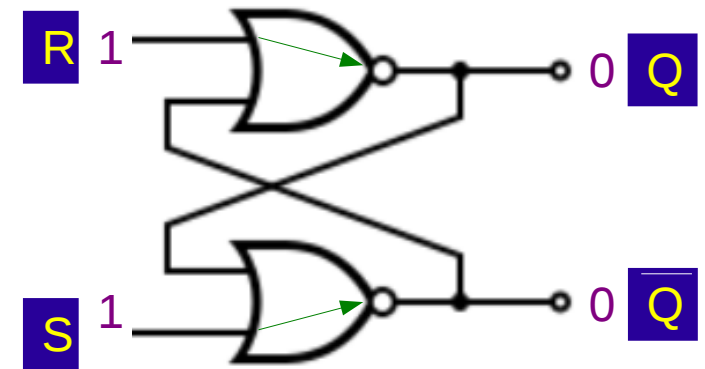
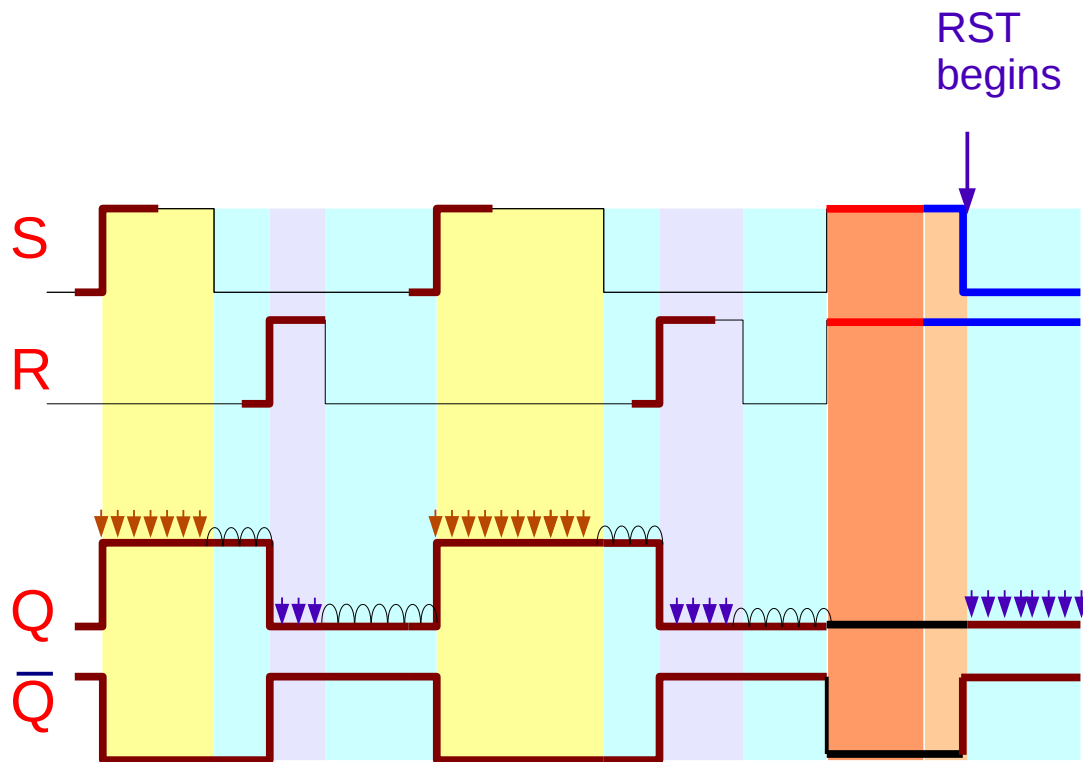
# NOR-based SR Latch



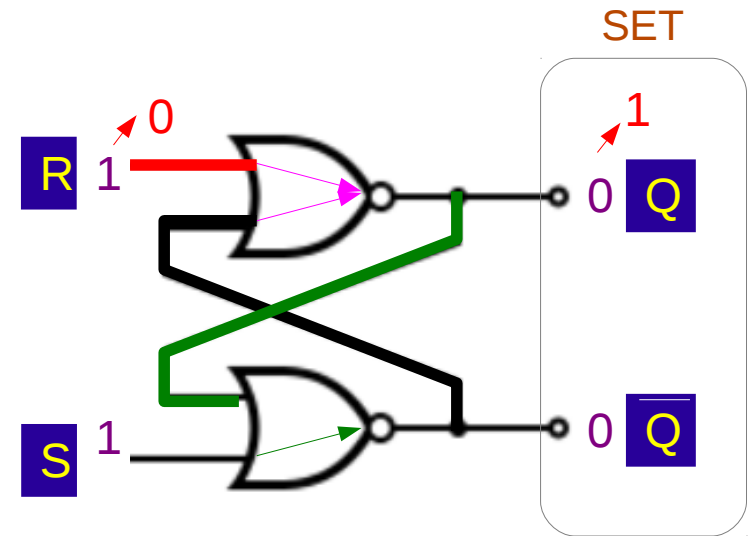
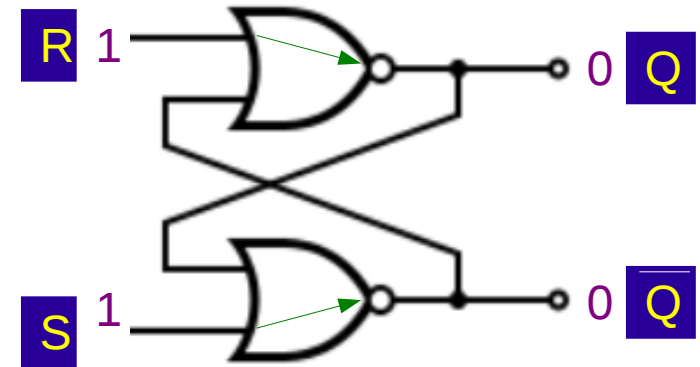
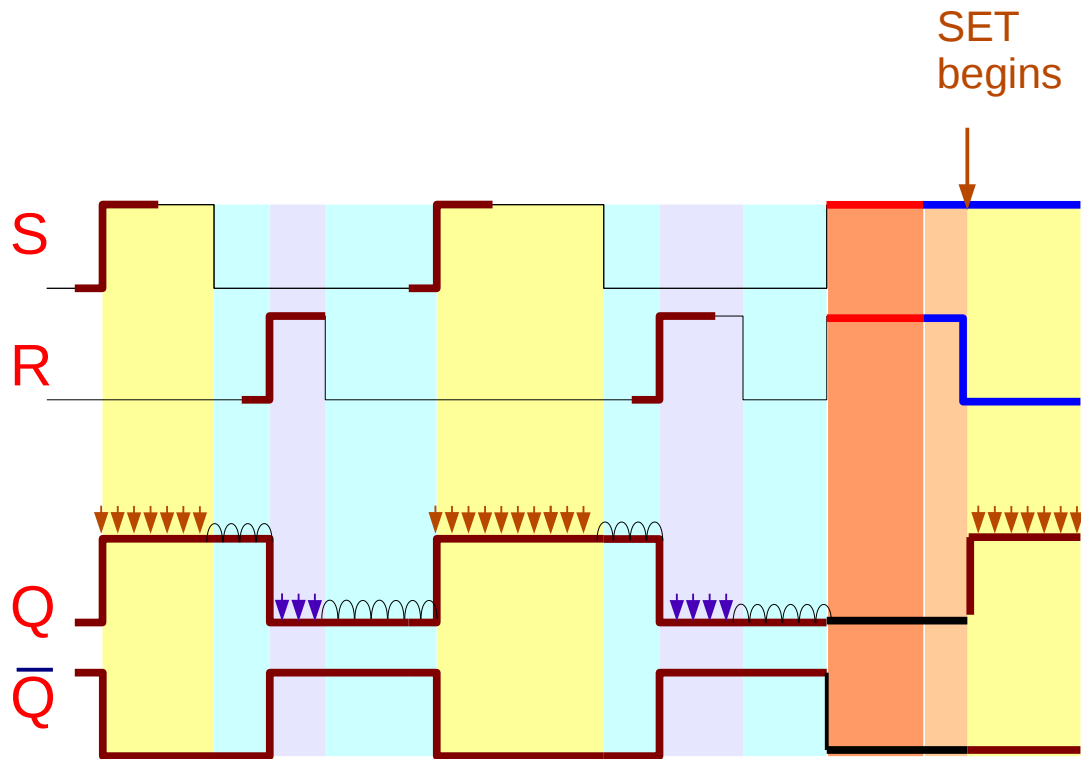
# Gated SR Latch (SR=11)



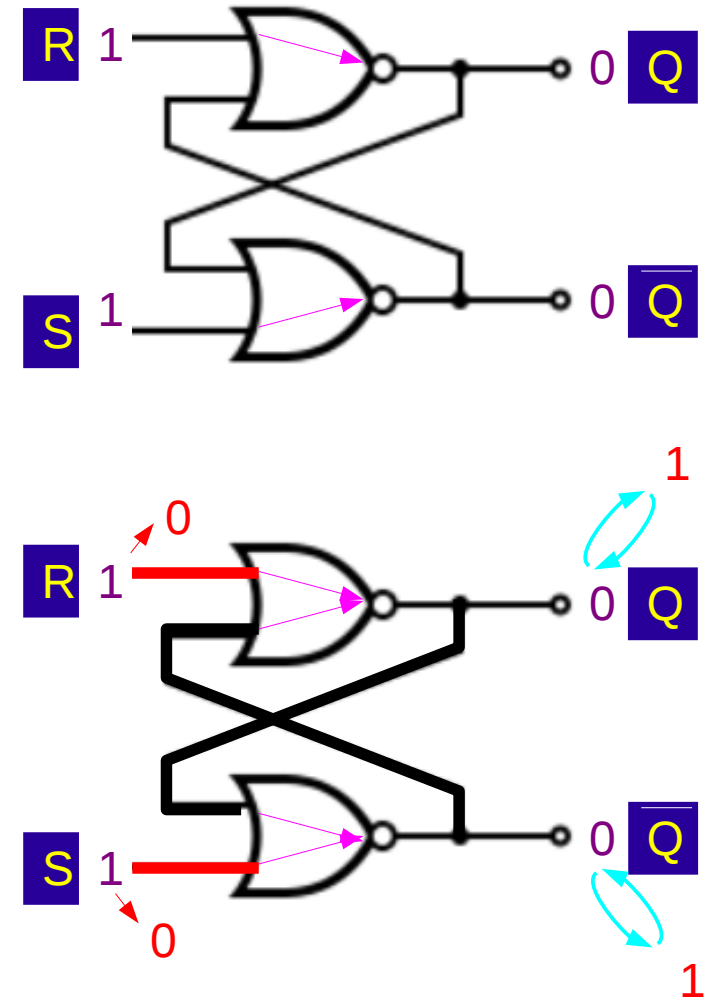
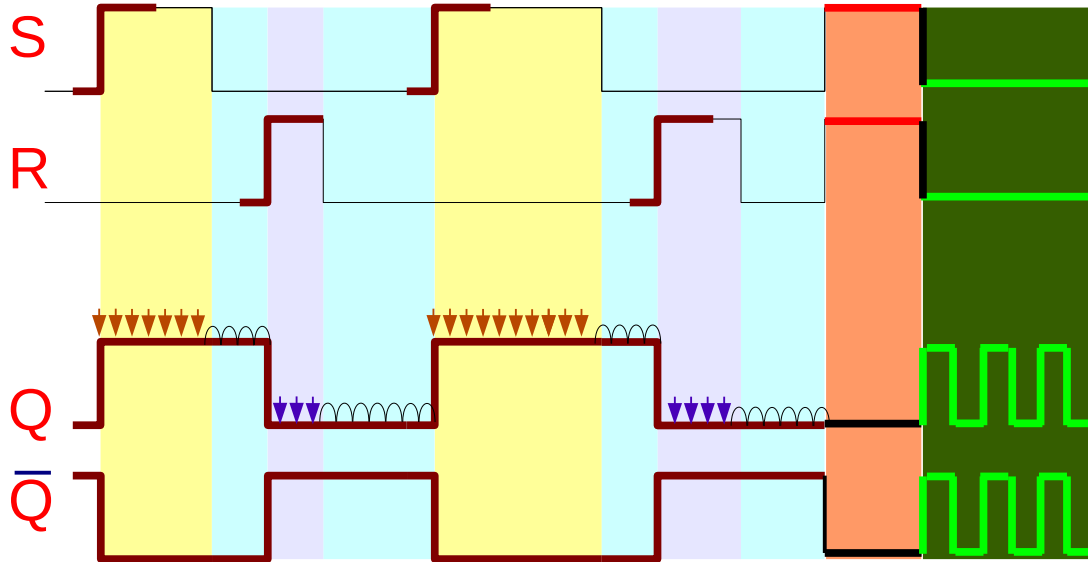
# Gated SR Latch (SR=11 to 01)



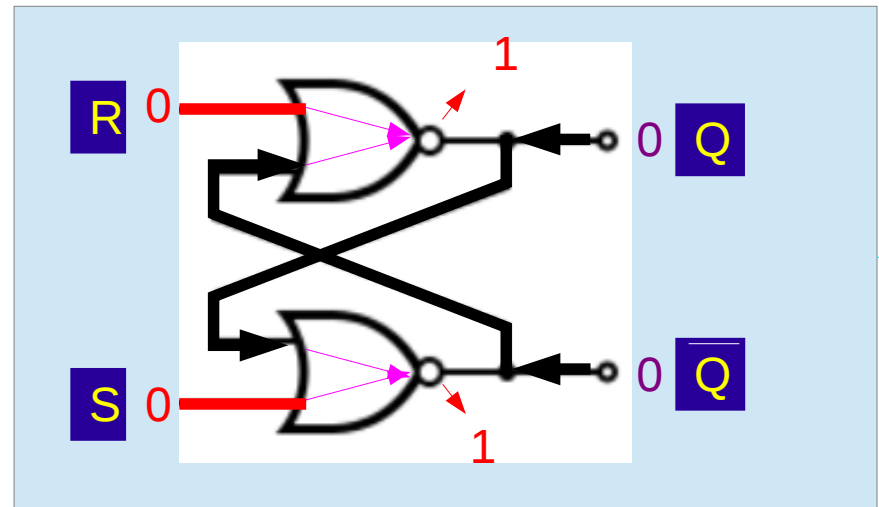
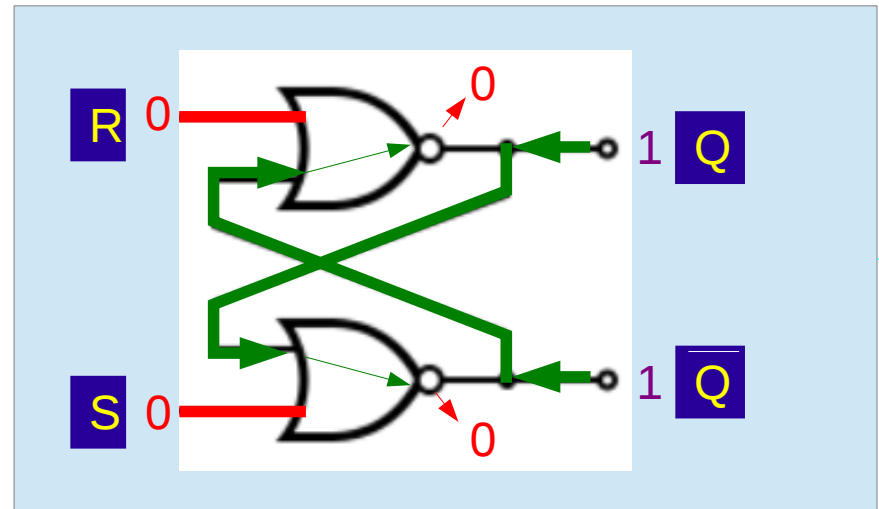
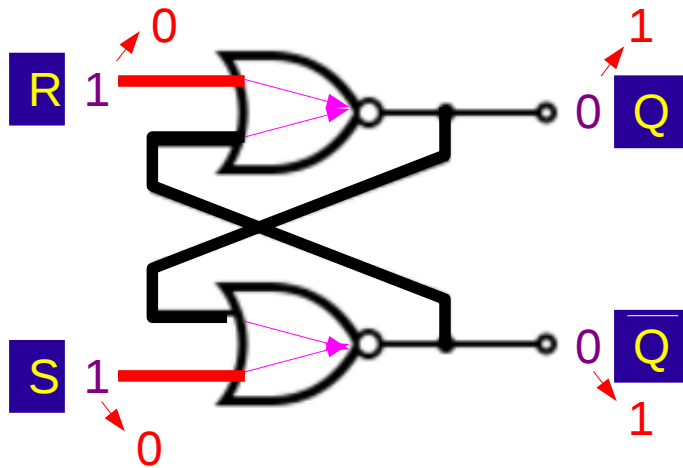
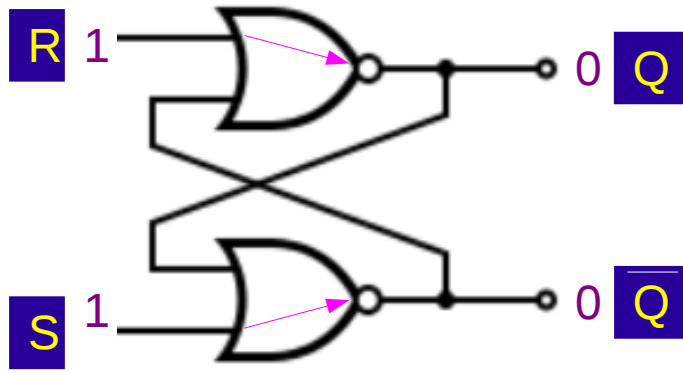
# Gated SR Latch (SR=11 to 10)



# Gated SR Latch (SR=11 to 00)

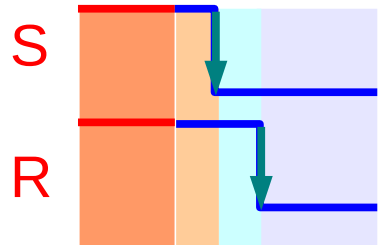


# Gated SR Latch Oscillation State

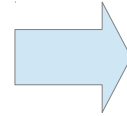




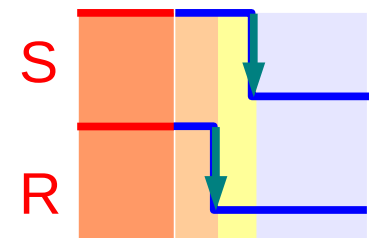
# Forbidden State Transition



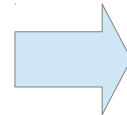
Forbidden St



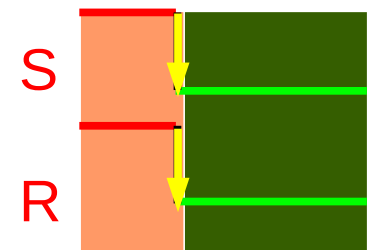
RESET, Hold



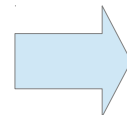
Forbidden St



SET, Hold



Forbidden St



Oscillation

## References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4<sup>th</sup> ed.