List of ARM microarchitectures

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This is a list of microarchitectures based on the ARM family of instruction sets designed by ARM Holdings and 3rd parties, sorted by version of the ARM instruction set, release and name. ARM provides a summary of the numerous vendors who implement ARM cores in their design.[1] Keil also provides a somewhat newer summary of vendors of ARM based processors.[2] ARM further provides a chart[3] displaying an overview of the ARM processor lineup with performance and functionality versus capabilities for the more recent ARM core families.

Contents

ARM cores

Designed by ARM

ARM family	ARM architecture	ARM core	Feature	Cache (I / D), MMU	Typical MIPS @ MHz
ARM1	ARMv1	ARM1	First implementation	None	
ARM2	ARMv2	ARM2	ARMv2 added the MUL (multiply) instruction	None	4 MIPS @ 8 MHz 0.33 DMIPS/MHz
	ARMv2a	ARM250	Integrated MEMC (MMU), graphics and I/O processor. ARMv2a added the SWP and SWPB (swap) instructions	None, MEMC1a	7 MIPS @ 12 MHz
ARM3	ARMv2a	ARM3	First integrated memory cache	4 KB unified	12 MIPS @ 25 MHz 0.50 DMIPS/MHz
ARM6	ARMv3	ARM60	ARMv3 first to support 32-bit memory address space (previously 26-bit)	None	10 MIPS @ 12 MHz
		ARM600	As ARM60, cache and coprocessor bus (for FPA10 floating-point unit)	4 KB unified	28 MIPS @ 33 MHz
		ARM610	As ARM60, cache, no coprocessor bus	4 KB unified	17 MIPS @ 20 MHz 0.65 DMIPS/MHz
ARM7	ARMv3	ARM700		8 KB unified	40 MHz
		ARM710	As ARM700, no coprocessor bus	8 KB unified	40 MHz
		ARM710a	As ARM710	8 KB unified	40 MHz 0.68 DMIPS/MHz
ARM7TDMI	ARMv4T	ARM7TDMI(-S)	3-stage pipeline, Thumb, ARMv4 first to drop legacy ARM 26-bit addressing	none	15 MIPS @ 16.8 MHz 63 DMIPS @ 70 MHz
		ARM710T	As ARM7TDMI, cache	8 KB unified, MMU	36 MIPS @ 40 MHz
		ARM720T	As ARM7TDMI, cache	8 KB unified, MMU with Fast Context Switch Extension	60 MIPS @ 59.8 MHz
		ARM740T	As ARM7TDMI, cache	MPU	
ARM7EJ	ARMv5TEJ	ARM7EJ-S	5-stage pipeline, Thumb, Jazelle DBX, Enhanced DSP instructions	none	

ARM8	ARMv4	ARM810[4][5]	5-stage pipeline, static branch prediction, double-bandwidth memory	8 KB unified, MMU	84 MIPS @ 72 MHz 1.16 DMIPS/MHz
ARM9TDMI	ARMv4T	ARM9TDMI	5-stage pipeline, Thumb	none	
		ARM920T	As ARM9TDMI, cache	16 KB / 16 KB, MMU with FCSE (Fast Context Switch Extension)[6]	200 MIPS @ 180 MHz
		ARM922T	As ARM9TDMI, caches	8 KB / 8 KB, MMU	
		ARM940T	As ARM9TDMI, caches	4 KB / 4 KB, MPU	
ARM9E	ARMv5TE	ARM946E-S	Thumb, Enhanced DSP instructions, caches	variable, tightly coupled memories, MPU	
		ARM966E-S	Thumb, Enhanced DSP instructions	no cache, TCMs	
		ARM968E-S	As ARM966E-S	no cache, TCMs	
	ARMv5TEJ	ARM926EJ-S	Thumb, Jazelle DBX, Enhanced DSP instructions	variable, TCMs, MMU	220 MIPS @ 200 MHz
	ARMv5TE	ARM996HS	Clockless processor, as ARM966E-S	no caches, TCMs, MPU	
ARM10E	ARMv5TE	ARM1020E	6-stage pipeline, Thumb, Enhanced DSP instructions, (VFP)	32 KB / 32 KB, MMU	
		ARM1022E	As ARM1020E	16 KB / 16 KB, MMU	
	ARMv5TEJ	ARM1026EJ-S	Thumb, Jazelle DBX, Enhanced DSP instructions, (VFP)	variable, MMU or MPU	
ARM11	ARMv6	ARM1136J(F)-S[7]	8-stage pipeline, SIMD, Thumb, Jazelle DBX, (VFP), Enhanced DSP instructions	variable, MMU	740 @ 532–665 MHz (i.MX31 SoC), 400–528 MHz
	ARMv6T2	ARM1156T2(F)-S	8-stage pipeline, SIMD, Thumb-2, (VFP), Enhanced DSP instructions	variable, MPU	

	ARMv6Z	ARM1176JZ(F)-S	As ARM1136EJ(F)-S	variable, MMU + TrustZone	965 DMIPS @ 772 MHz, up to 2,600 DMIPS with four processors[8]
	ARMv6K	ARM11 MPCore	As ARM1136EJ(F)-S, 1–4 core SMP	variable, MMU	
SecurCore	ARMv6-M	SC000			0.9 DMIPS/MHz
	ARMv4T	SC100			
	ARMv7-M	SC300			1.25 DMIPS/MHz
Cortex-M	ARMv6-M	Cortex-M0[9]	Microcontroller profile, Thumb + Thumb-2 subset (BL, MRS, MSR, ISB, DSB, DMB),[10] hardware multiply instruction (optional small), optional system timer, optional bit-banding memory	Optional cache, No TCM, No MPU	0.84 DMIPS/MHz
		Cortex-M0+[11]	Microcontroller profile, Thumb + Thumb-2 subset (BL, MRS, MSR, ISB, DSB, DMB),[10] hardware multiply instruction (optional small), optional system timer, optional bit-banding memory	Optional cache, No TCM, optional MPU with 8 regions	0.93 DMIPS/MHz
		Cortex-M1[12]	Microcontroller profile, Thumb + Thumb-2 subset (BL, MRS, MSR, ISB, DSB, DMB),[10] hardware multiply instruction (optional small), OS option adds SVC / banked stack pointer, optional system timer, no bit-banding memory	Optional cache, 0-1024 KB I-TCM, 0-1024 KB D-TCM, No MPU	136 DMIPS @ 170 MHz,[13] (0.8 DMIPS/MHz FPGA-dependent)[14]
	ARMv7-M	Cortex-M3[15]	Microcontroller profile, Thumb / Thumb-2, hardware multiply and divide instructions, optional bit-banding memory	Optional cache, No TCM, optional MPU with 8 regions	1.25 DMIPS/MHz
	ARMv7E-M	Cortex-M4[16]	Microcontroller profile, Thumb / Thumb-2 / DSP / optional FPv4 single-precision FPU, hardware multiply and divide instructions, optional bit-banding memory	Optional cache, No TCM, optional MPU with 8 regions	1.25 DMIPS/MHz
Cortex-R	ARMv7-R	Cortex-R4[17]	Real-time profile, Thumb / Thumb-2 / DSP / optional VFPv3 FPU, hardware multiply and	0–64 KB / 0–64 KB, 0–2 of 0–8 MB TCM,	

			optional divide instructions, optional parity & ECC for internal buses / cache / TCM, 8-stage pipeline dual-core running lockstep with fault logic	opt MPU with 8/12 regions	
		Cortex-R5 (MPCore)[18]	Real-time profile, Thumb / Thumb-2 / DSP / optional VFPv3 FPU and precision, hardware multiply and optional divide instructions, optional parity & ECC for internal buses / cache / TCM, 8-stage pipeline dual-core running lock-step with fault logic / optional as 2 independent cores, low-latency peripheral port (LLPP), accelerator coherency port (ACP)[19]	0–64 KB / 0–64 KB, 0–2 of 0–8 MB TCM, opt MPU with 12/16 regions	
		Cortex-R7 (MPCore)[20]	Real-time profile, Thumb / Thumb-2 / DSP / optional VFPv3 FPU and precision, hardware multiply and optional divide instructions, optional parity & ECC for internal buses / cache / TCM, 11-stage pipeline dual-core running lock-step with fault logic / out-of-order execution / dynamic register renaming / optional as 2 independent cores, low-latency peripheral port (LLPP), ACP[19]	0–64 KB / 0–64 KB, ? of 0–128 KB TCM, opt MPU with 16 regions	
Cortex-A	ARMv7-A	Cortex-A5[21]	Application profile, ARM / Thumb / Thumb-2 / DSP / SIMD / Optional VFPv4-D16 FPU / Optional NEON / Jazelle RCT and DBX, 1–4 cores / optional MPCore, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	4-64 KB / 4-64 KB L1, MMU + TrustZone	1.57 DMIPS/MHz per core
		Cortex-A7 MPCore[22]	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4-D16 FPU / NEON / Jazelle RCT and DBX / Hardware virtualization, in-order execution, superscalar, 1–4 SMP cores, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt	32 KB / 32 KB L1, 0–4 MB L2, MMU + TrustZone	1.9 DMIPS/MHz per core

			controller (GIC), ACP, architecture and feature set are identical to A15, 8-10 stage pipeline, low-power design[23]		
		Cortex-A8[24]	Application profile, ARM / Thumb / Thumb-2 / VFPv3 FPU / NEON / Jazelle RCT and DAC, 13-stage superscalar pipeline	16-32 KB / 16–32 KB L1, 0–1 MB L2 opt ECC, MMU + TrustZone	Up to 2000 (2.0 DMIPS/MHz in speed from 600 MHz to greater than 1 GHz)
		Cortex-A9 MPCore[25]	Application profile, ARM / Thumb / Thumb-2 / DSP / Optional VFPv3 FPU / Optional NEON / Jazelle RCT and DBX, out-of-order speculative issue superscalar, 1–4 SMP cores, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	16–64 KB / 16–64 KB L1, 0–8 MB L2 opt parity, MMU + TrustZone	2.5 DMIPS/MHz per core, 10,000 DMIPS @ 2 GHz on Performance Optimized TSMC 40G (dual-core)
		Cortex-A12[26]	Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	32-64 KB / 32 KB L1, 256 KB-8 MB L2	3.0 DMIPS/MHz per core
		Cortex-A15 MPCore[27]	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / Fused MAC / Jazelle RCT / Hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP, 15-24 stage pipeline[23]	32 KB w/parity / 32 KB w/ECC L1, 0–4 MB L2, L2 has ECC, MMU + TrustZone	At least 3.5 DMIPS/MHz per core (up to 4.01 DMIPS/MHz depending on implementation)[28]
		Cortex-A17 MPCore	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / Fused MAC / Jazelle RCT / Hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, Large Physical	MMU + TrustZone	

			Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP		
Cortex-A50	ARMv8-A	Cortex-A53[29]	Application profile, AArch32 and AArch64, 1-4 SMP cores, Trustzone, NEON advanced SIMD, VFPv4, hardware virtualization, dual issue, in-order pipeline	8-64 KB w/parity / 8-64 KB w/ECC L1 per core, 128 KB-2 MB L2 shared, 40-bit physical addresses	2.3 DMIPS/MHz
		Cortex-A57[30]	Application profile, AArch32 and AArch64, 1-4 SMP cores, Trustzone, NEON advanced SIMD, VFPv4, hardware virtualization, multi-issue, deeply out-of-order pipeline	48 KB w/DED parity / 32 KB w/ECC L1 per core, 512 KB-2 MB L2 shared, 44-bit physical addresses	At least 4.1 DMIPS/MHz per core (up to 4.76 DMIPS/MHz depending on implementation)
ARM family	**ARM architecture**	**ARM core**	**Feature**	**Cache (I / D), MMU**	**Typical MIPS @ MHz**

Designed by third parties

These cores implement the ARM instruction set, and were developed independently by companies with an architectural license from ARM.

Family	Instruction set	Microarchitecture	Feature	Cache (I / D), MMU	Typical MIPS @ MHz
StrongARM	ARMv4	SA-110	5-stage pipeline	16 KB / 16 KB, MMU	100–206 MHz 1.0 DMIPS/MHz
		SA-1100	derivative of the SA-110	16 KB / 8 KB, MMU	
Faraday[31]	ARMv4	FA510	6-stage pipeline	up to 32 KB / 32 KB Cache, MPU	1.26 DMIPS/MHz 100–200 MHz
		FA526		up to 32 KB / 32 KB Cache, MMU	1.26 MIPS/MHz 166-300 MHz
		FA626	8-stage pipeline	32 KB / 32 KB Cache, MMU	1.35 DMIPS/MHz 500 MHz
	ARMv5TE	FA606TE	5-stage pipeline	no cache, no MMU	1.22 DMIPS/MHz 200 MHz
		FA626TE	8-stage pipeline	32 KB / 32 KB Cache, MMU	1.43 MIPS/MHz 800 MHz
		FMP626TE	8-stage pipeline, SMP		1.43 MIPS/MHz 500 MHz
		FA726TE	13 stage pipeline, dual issue		2.4 DMIPS/MHz 1000 MHz
XScale	ARMv5TE	XScale	7-stage pipeline, Thumb, Enhanced DSP instructions	32 KB / 32 KB, MMU	133–400 MHz
		Bulverde	Wireless MMX, Wireless SpeedStep added	32 KB / 32 KB, MMU	312–624 MHz
		Monahans[32]	Wireless MMX2 added	32 KB / 32 KB (L1), optional L2 cache up to 512 KB, MMU	up to 1.25 GHz
Marvell Sheeva	ARMv5	Feroceon	5-8 stage pipeline, single-issue	16 KB / 16 KB, MMU	600–2000 MHz
		Jolteon	5-8 stage pipeline, dual-issue	32 KB / 32 KB, MMU	
		PJ1 (Mohawk)	5-8 stage pipeline, single-issue, Wireless MMX2	32 KB / 32 KB, MMU	1.46 DMIPS/MHz 1.06 GHz

	ARMv6 / ARMv7-A	PJ4	6-9 stage pipeline, dual-issue, Wireless MMX2, SMP	32 KB / 32 KB, MMU	2.41 DMIPS/MHz 1.6 GHz
Snapdragon	ARMv7-A	Scorpion[33]	1 or 2 cores. ARM / Thumb / Thumb-2 / DSP / SIMD / VFPv3 FPU / NEON (128-bit wide)	256 KB L2 per core	2.1 DMIPS/MHz per core
		Krait[33]	1, 2, or 4 cores. ARM / Thumb / Thumb-2 / DSP / SIMD / VFPv4 FPU / NEON (128-bit wide)	4 KB / 4 KB L0, 16 KB / 16 KB L1, 512 KB L2 per core	3.3 DMIPS/MHz per core
Apple A6, Apple A6X	ARMv7-A	Swift[34]	2 cores. ARM / Thumb / Thumb-2 / DSP / SIMD / VFPv4 FPU / NEON	L1: 32 KB / 32 KB, L2: 1 MB	3.5 DMIPS/MHz per core
Apple A7	ARMv8-A	Cyclone	2 cores. ARM / Thumb / Thumb-2 / DSP / SIMD / VFPv4 FPU / NEON / TrustZone / AArch64	L1: 64 KB / 64 KB, L2: 1 MB	
X-Gene	ARMv8-A	X-Gene	64-bit, quad issue, SMP	Cache, MMU, virtualization	3 GHz
Denver	ARMv8-A	Denver	64-bit	128KB I/64KB D	Up to 2.5GHz
ThunderX	ARMv8-A	ThunderX	8-16 / 24-48 cores (×2 w/two chips). 64-bit		up to 2.5 GHz

ARM core timeline

The following tables lists each core by the year it was announced.[35][36]

Year	ARM7 cores
1998	ARM7TDMI(-S)

Year	ARM8 cores
1996	ARM810

Year	ARM9 cores
1997	ARM9TDMI
2003	ARM966E-S
2003	ARM968E-S
2006	ARM996HS

Year	ARM11 cores
2002	ARM1136J(F)-S
2003	ARM1156T2(F)-S ARM1176JZ(F)-S

Year	Cortex cores		
	Embedded	Real-time	Application
2004	Cortex-M3		
2005			Cortex-A8
2007	Cortex-M1		Cortex-A9
2009	Cortex-M0		Cortex-A5
2010	Cortex-M4		Cortex-A15
2011		Cortex-R4 Cortex-R5 Cortex-R7	Cortex-A7
2012	Cortex-M0+		Cortex-A53 Cortex-A57
2013			Cortex-A12
2014			Cortex-A17

See also

- Comparison of ARMv7-A cores
- Comparison of ARMv8-A cores
- ARM architecture
- List of applications of ARM cores
- Comparison of current ARM cores

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Further reading

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- *The Definitive Guide to the ARM Cortex-M3 and Cortex-M4 Processors*; 3rd Edition; Joseph Yiu; Newnes; 600 pages; 2013; ISBN 978-0124080829.
- *The Definitive Guide to the ARM Cortex-M0*; 1st Edition; Joseph Yiu; Newnes; 552 pages; 2011; ISBN 978-0-12-385477-3. (Online Sample) (http://books.google.com/books?id=5OZblBzjsJ0C&printsec=frontcover&

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