

Finite State Machine (4B)

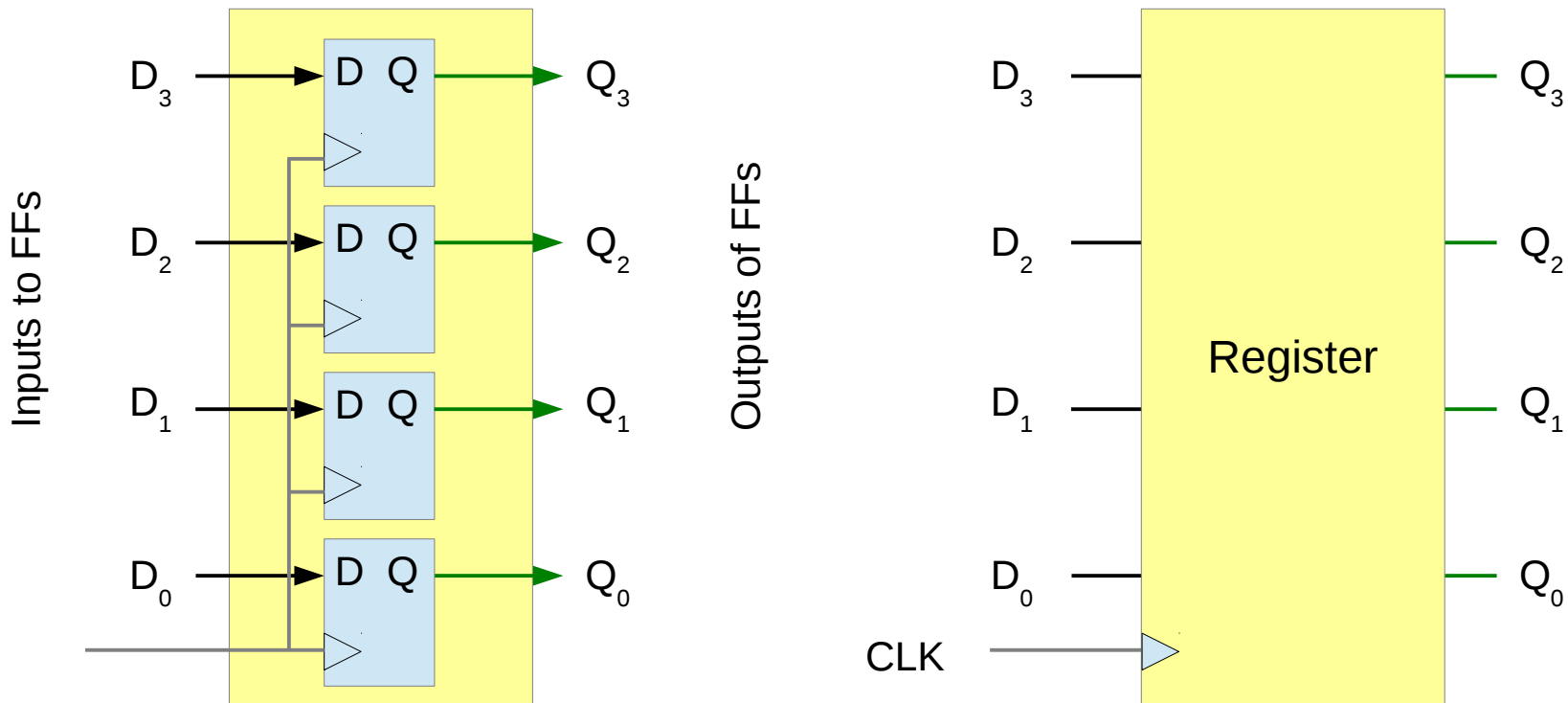
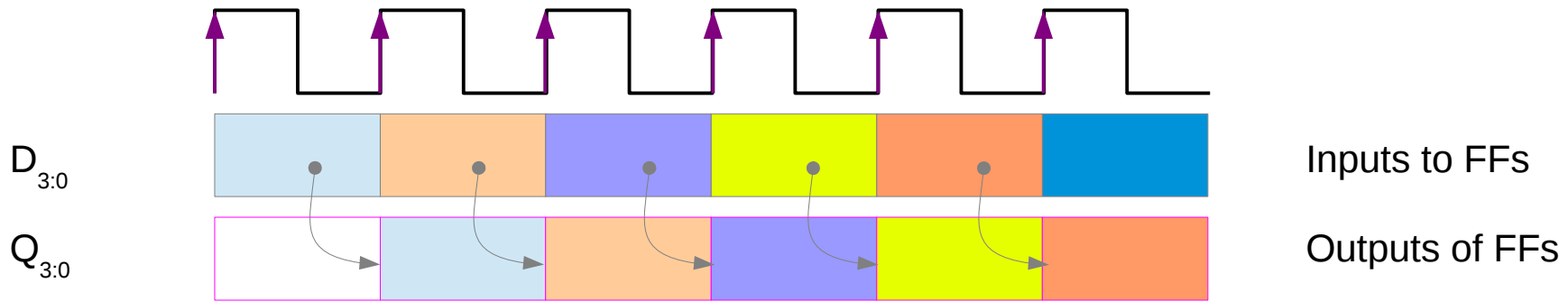
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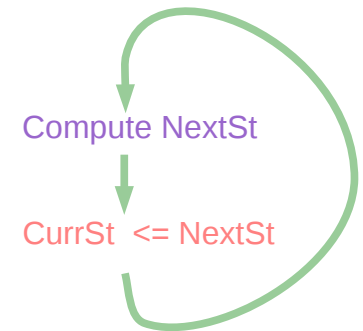
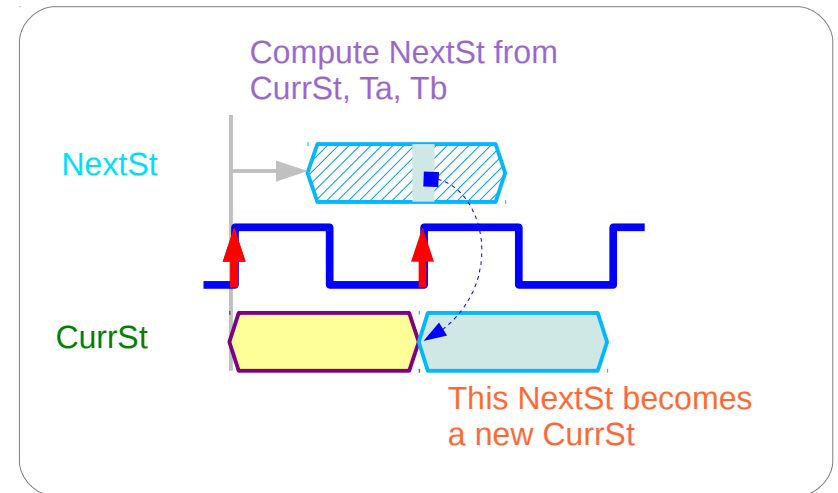
Please send corrections (or suggestions) to youngwlim@hotmail.com.

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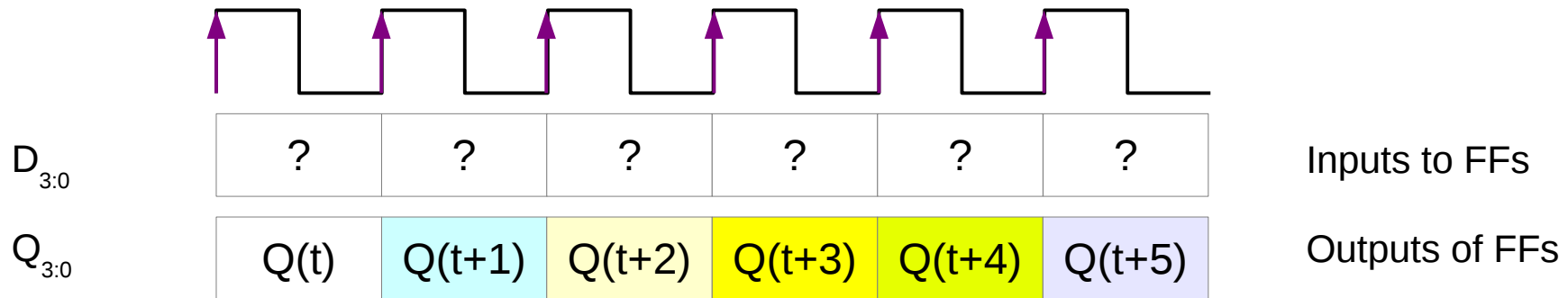
FF Timing (Ideal)



When NextSt becomes CurrSt

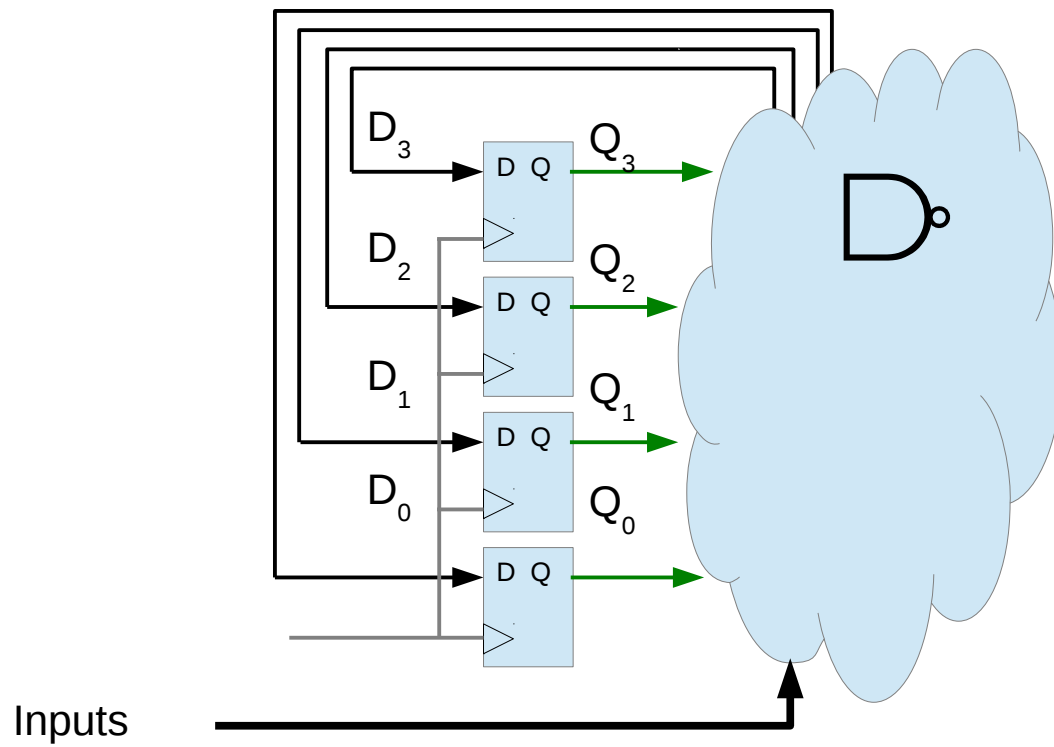


Finding FF Inputs



Inputs to FFs

Outputs of FFs



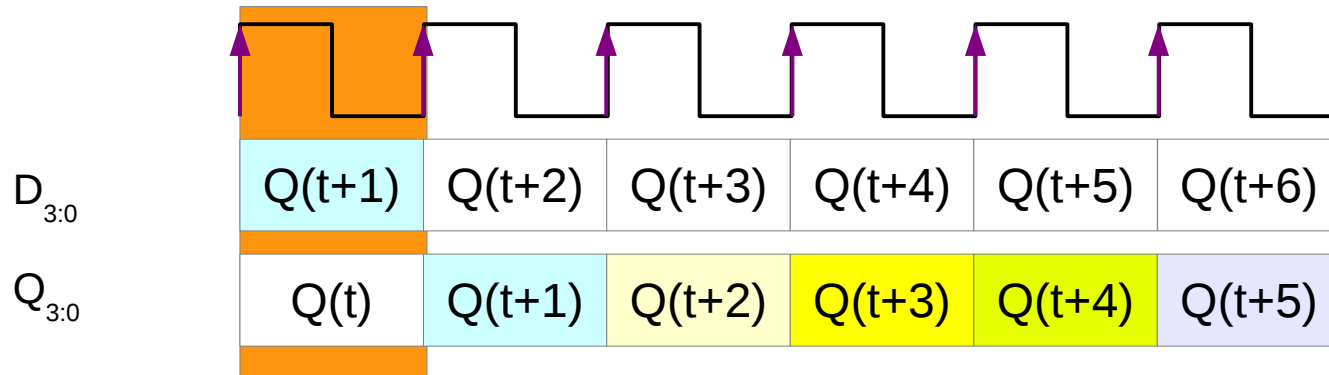
During the t^{th} clock edge period,

Compute the next state $Q(t+1)$ using the current state $Q(t)$ and other external inputs

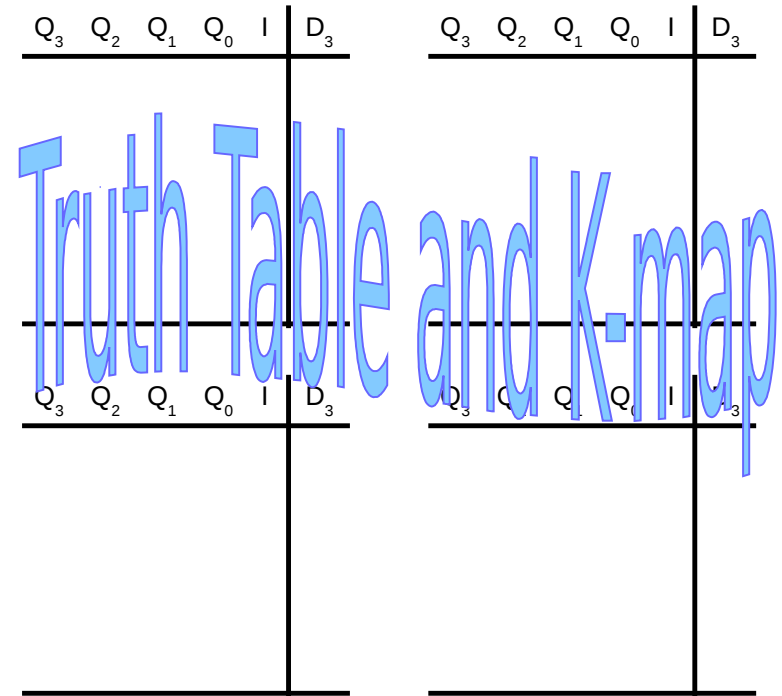
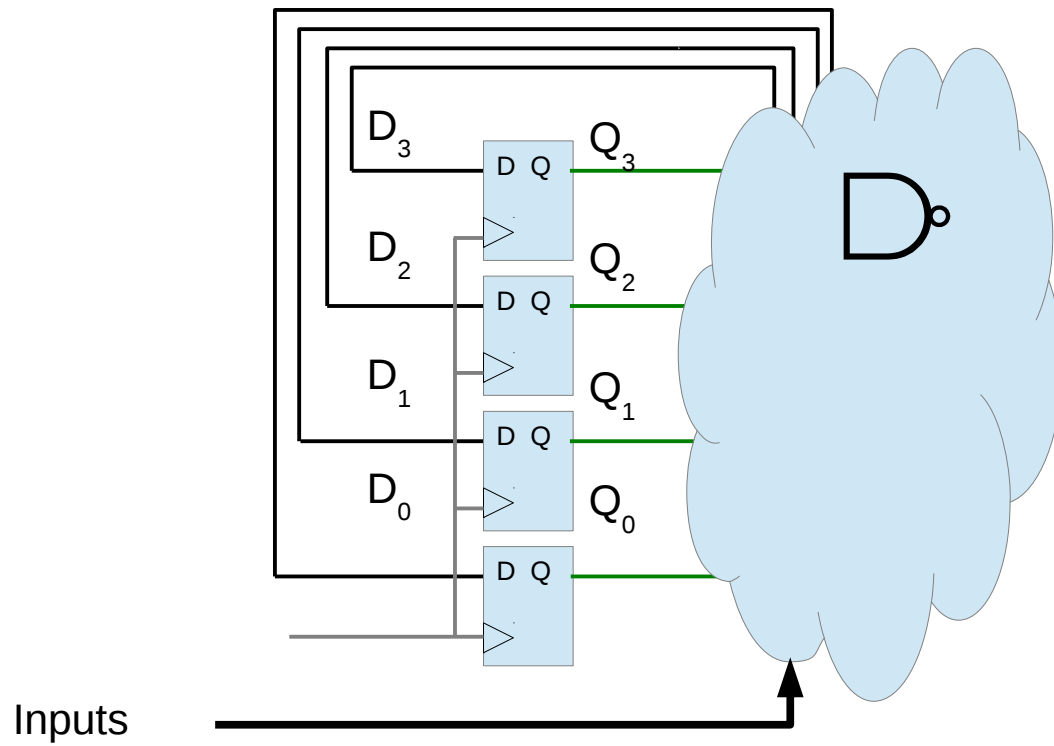
Place it to FF inputs

After the next clock edge, $(t+1)^{\text{th}}$, the **computed** next state $Q(t+1)$ becomes the current state

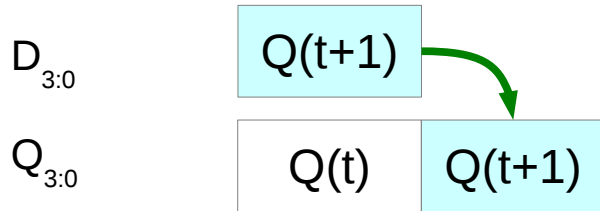
Method of Finding FF Inputs



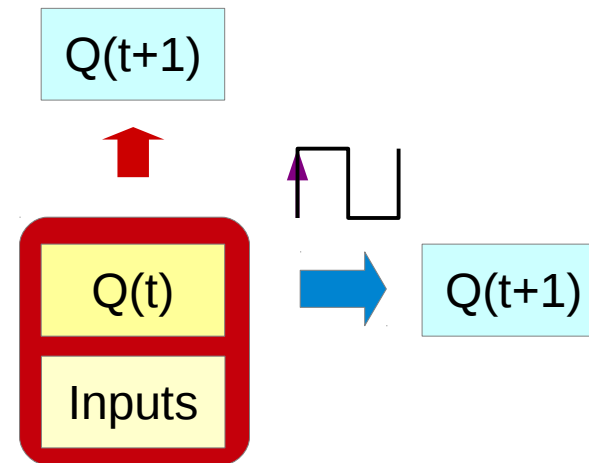
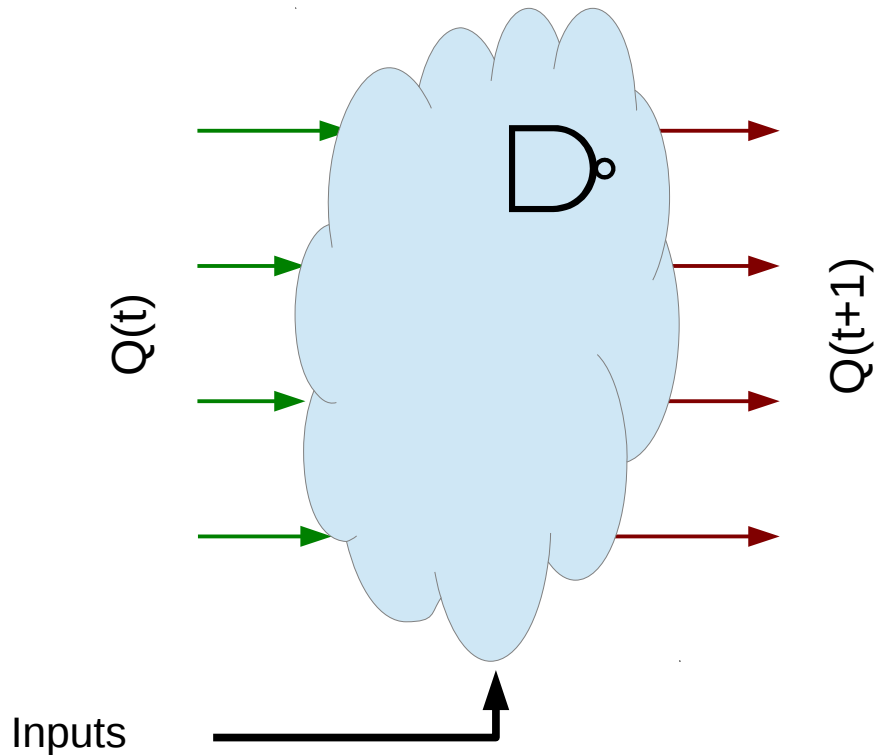
Find the **boolean functions** D_3, D_2, D_1, D_0 in terms of Q_3, Q_2, Q_1, Q_0 , and external inputs for all possible cases.



State Transition



Compute the next state using the current state and external inputs in the current clock cycle



After the next clock edge, the computed next state (FF Inputs) becomes the current state (FF Outputs)

Register Timing

References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4th ed.
- [3] D.M. Harris, S. L. Harris, "Digital Design and Computer Architecture"