

# Combinational Gates

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## Gate Level Design

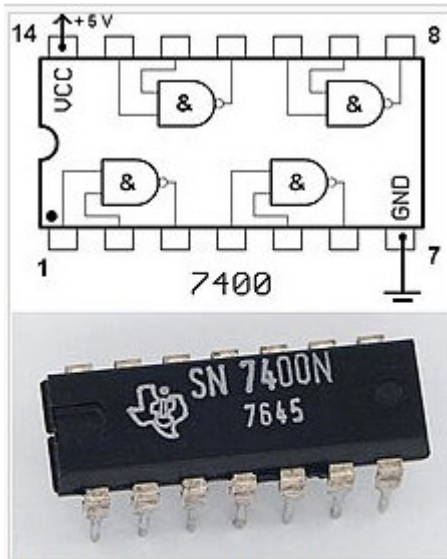
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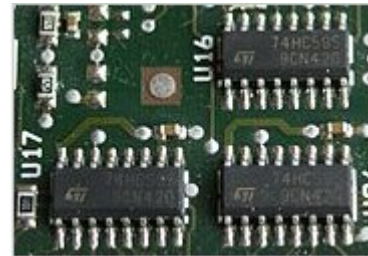
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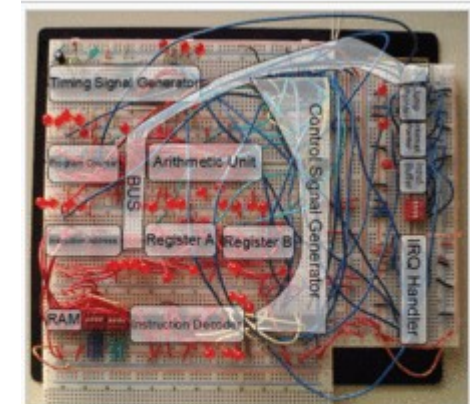
# TTL Gates : Building Blocks in 70's & 80's



The 7400 chip, containing four NANDs. The second line of numbers (7645) is a date code; this chip was manufactured in the 45th week of 1976.<sup>[1]</sup> The N suffix on the part number is a vendor-specific code indicating PDIP packaging.



Surface-mounted 74HC595 shift registers on a PCB. This IC is actually a high-speed CMOS circuit. If the product code had been 74HCT595, it would have been compatible with TTL signalling levels.



A 4-bit, 2 register, six-instruction computer made entirely of 74-series chips

[https://en.wikipedia.org/wiki/7400\\_series](https://en.wikipedia.org/wiki/7400_series)

# TTL Logic Gates

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- Buffers/Inverters/Drivers
- Digital Multiplexers
- Bus Switches
- Encoders
- Comparators
- Decoders/Demultiplexers
- Digital Comparators
- Gates
- Parity Generators/Checkers

## Combinational Logic Gates

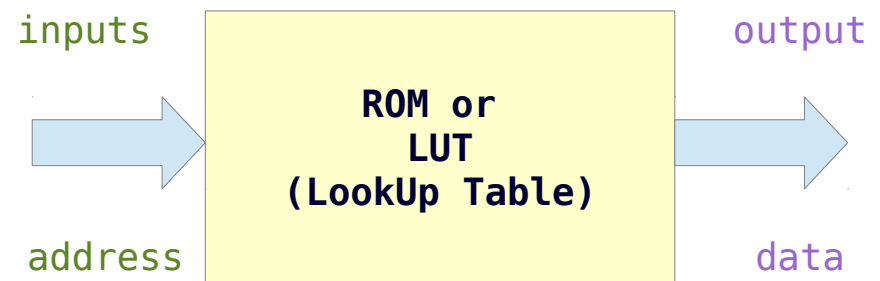
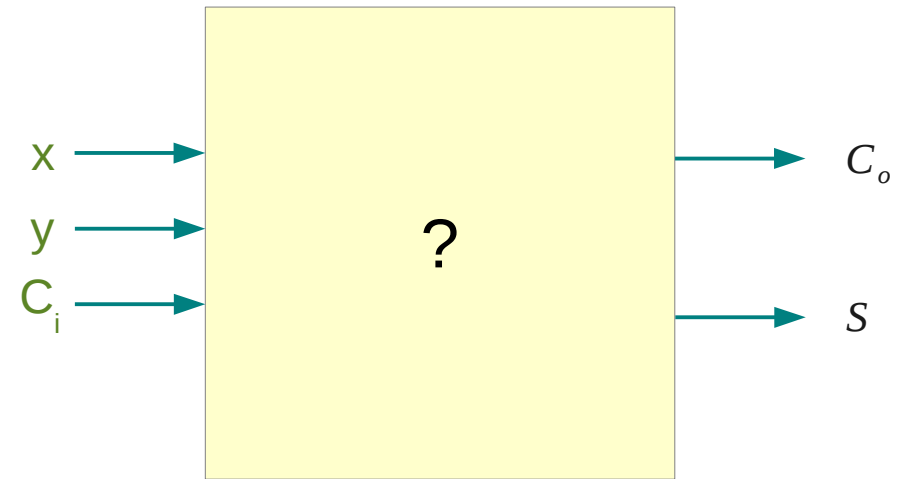
- Flip-Flops
- FIFO Registers
- Counters/Frequency Dividers
- Latches/Registered Drivers
- Shift Registers

## Sequential Logic Gates

# Truth Table

$x$	$y$	$C_i$	$C_o$	$S$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

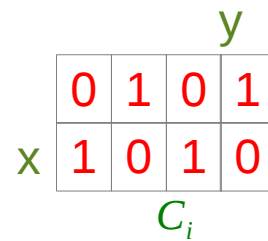
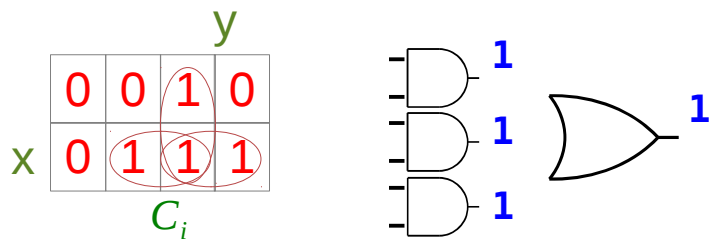
inputs      output



# SOP and K-Map Minimization

x	y	$C_i$	$C_o$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

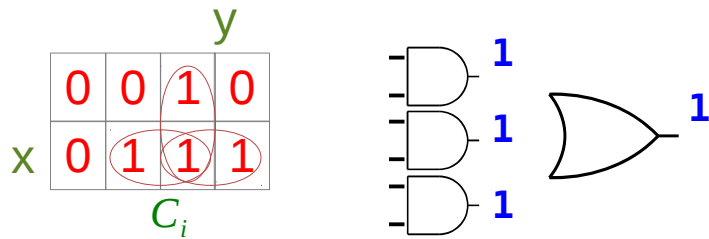
x	y	$C_i$	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



$$C_o = yC_i + xC_i + xy$$

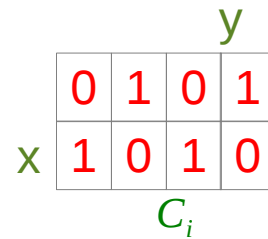
$$S = \bar{x}\bar{y}C_i + \bar{x}y\bar{C}_i + x\bar{y}\bar{C}_i + xyC_i$$

# Boolean Algebra



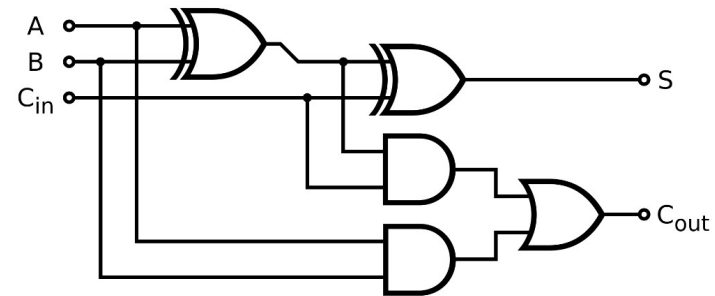
$$C_o = yC_i + xC_i + xy$$

$$\begin{aligned} C_o &= (x + y)C_i + xy \\ &= (\bar{x}y + x\bar{y} + xy)C_i + xy \\ &= (\bar{x}y + x\bar{y})C_i + xy(C_i + 1) \\ &= (x \oplus y)C_i + xy \end{aligned}$$



$$S = \bar{x}\bar{y}C_i + \bar{x}y\bar{C}_i + x\bar{y}\bar{C}_i + xyC_i$$

$$\begin{aligned} S &= (\bar{x}\bar{y} + xy)C_i + (\bar{x}y + x\bar{y})\bar{C}_i \\ &= \overline{(x \oplus y)}C_i + (x \oplus y)\bar{C}_i \\ &= (x \oplus y) \oplus C_i \end{aligned}$$



## References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_SOC\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design)
- [7] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Digital\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design)
- [8] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design)
- [9] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Architecture](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture)
- [10] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Organization](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization)