

# Gate Delay (3D)

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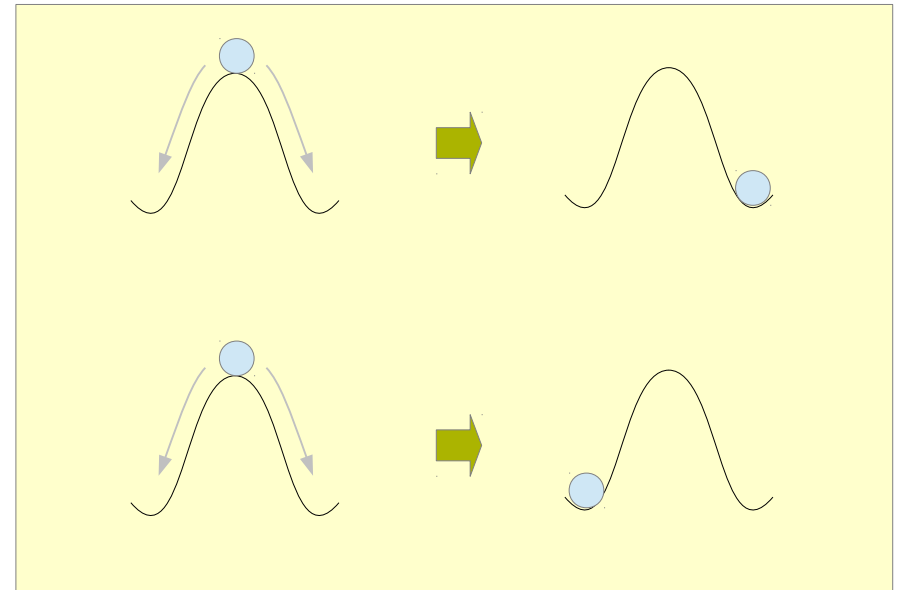
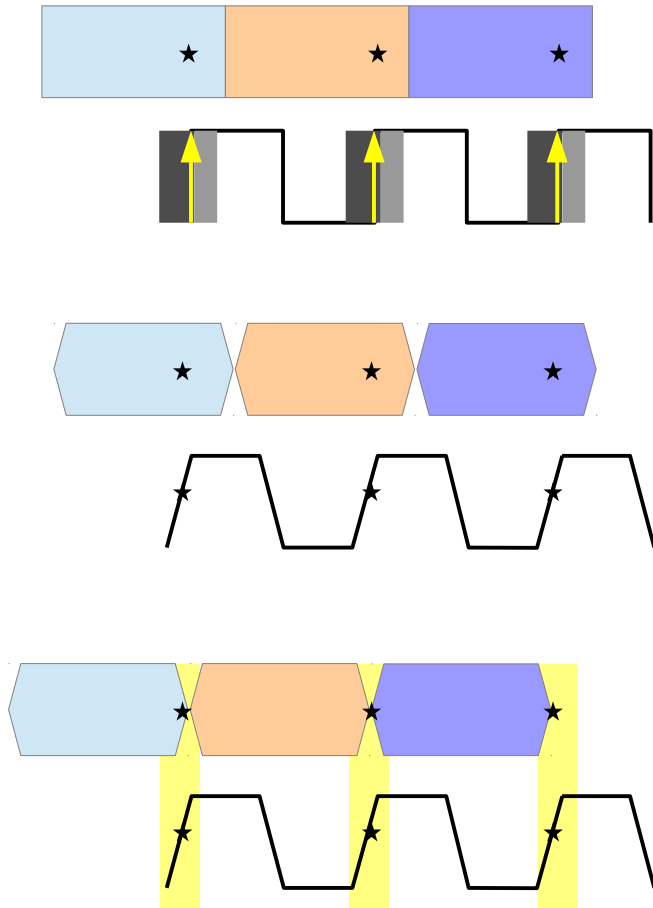
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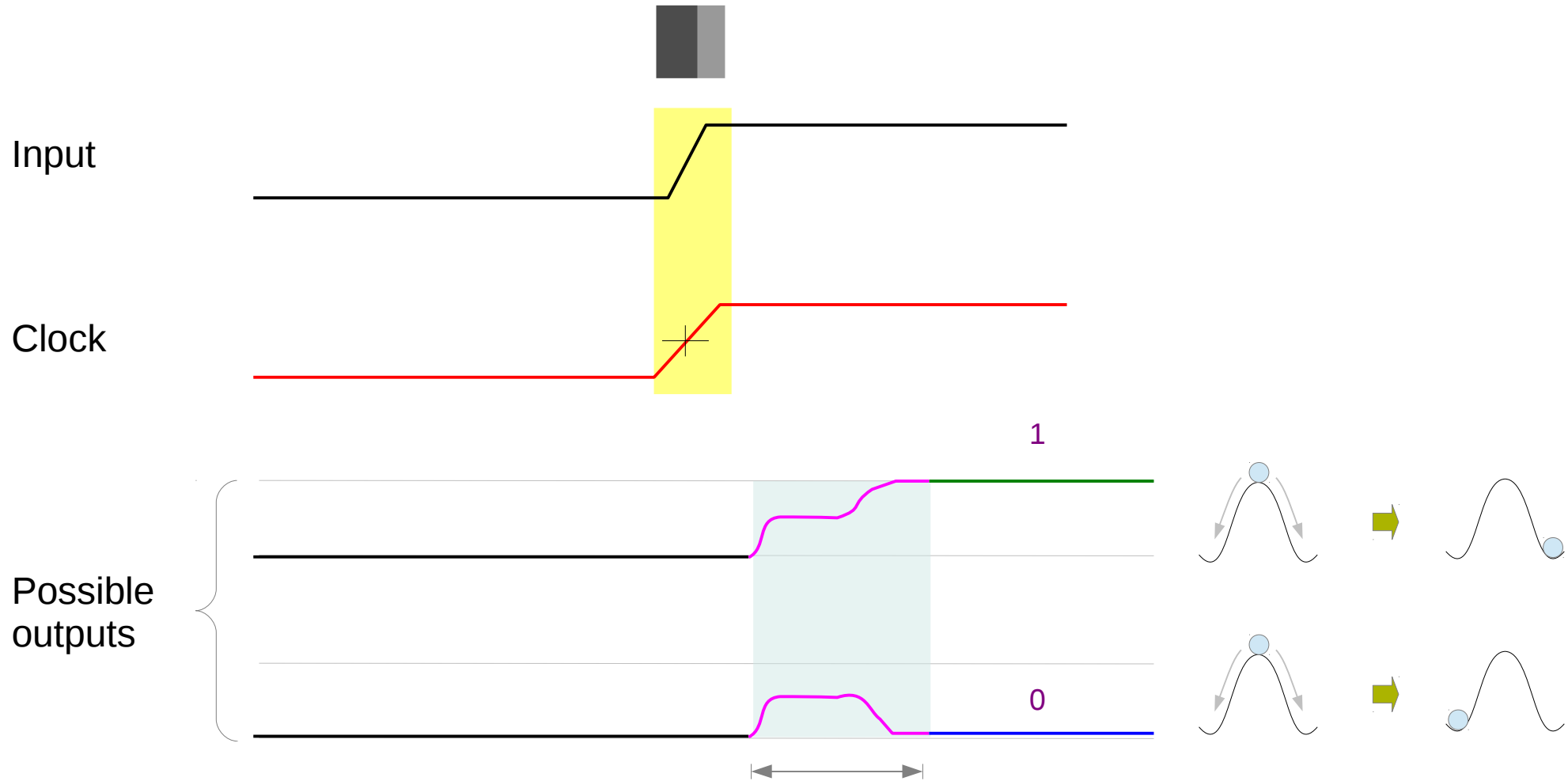
Please send corrections (or suggestions) to [youngwlim@hotmail.com](mailto:youngwlim@hotmail.com).

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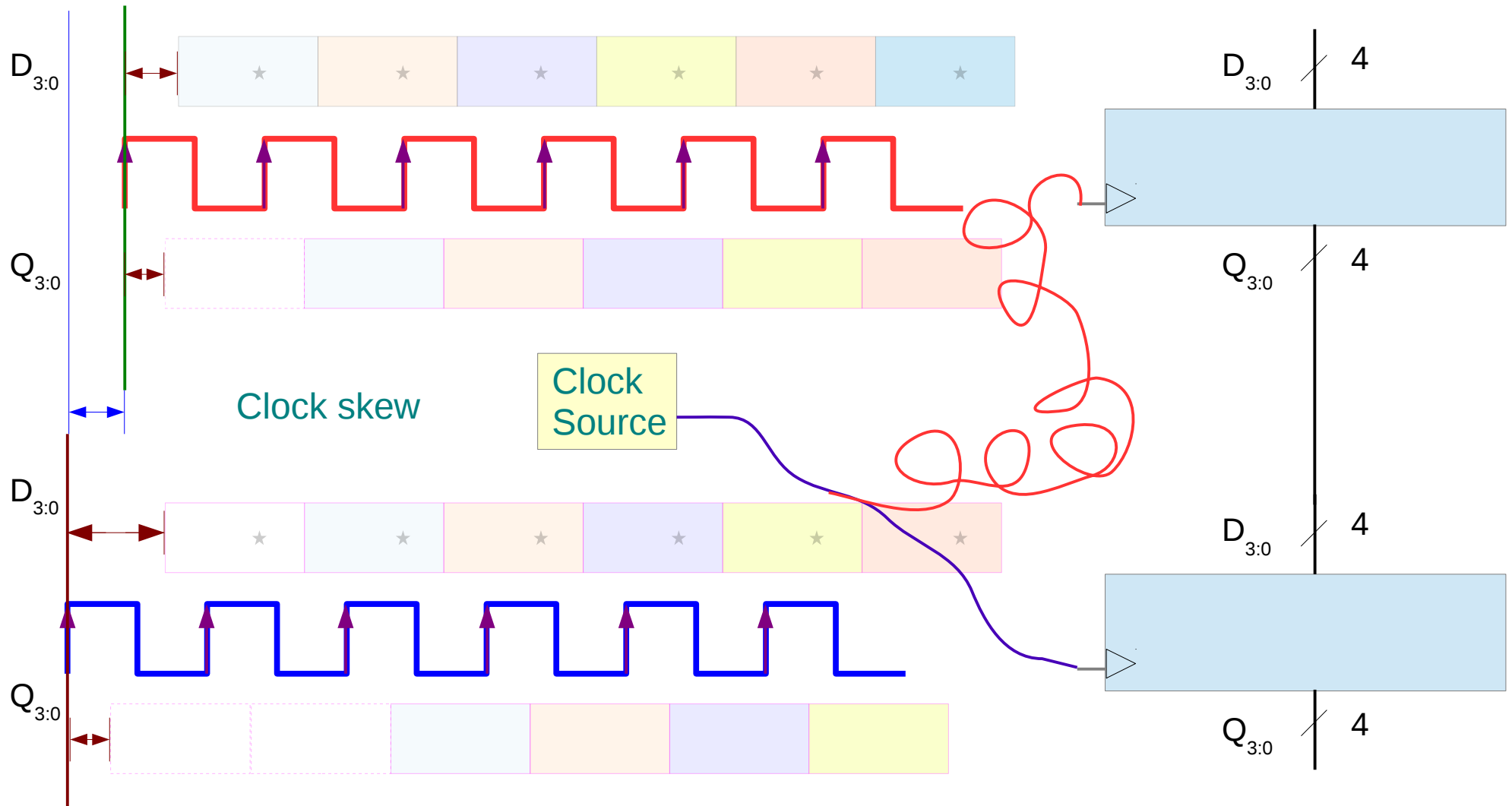
# Metastability



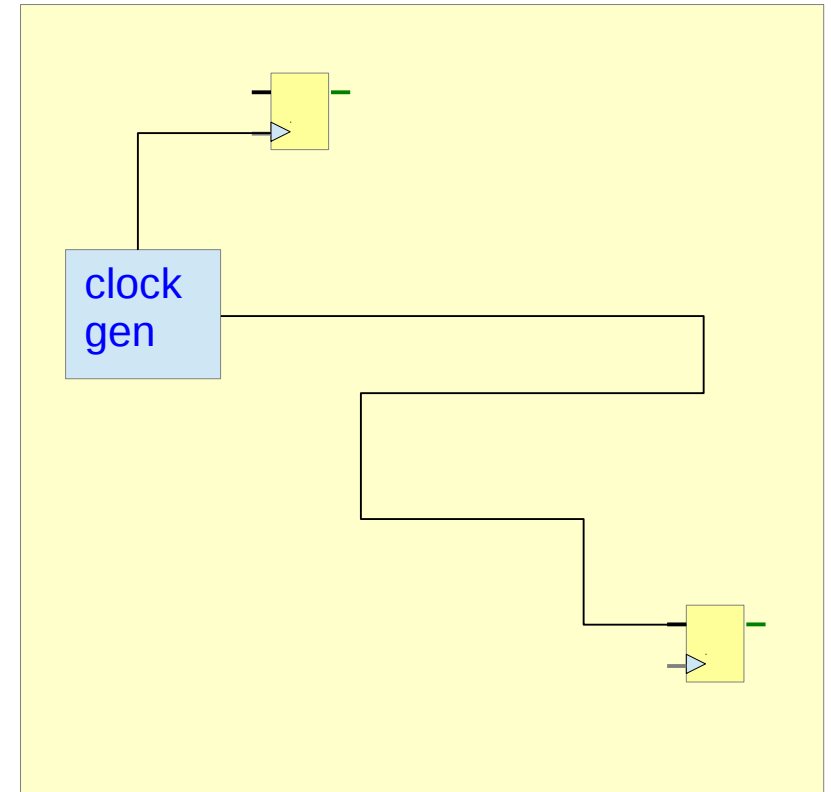
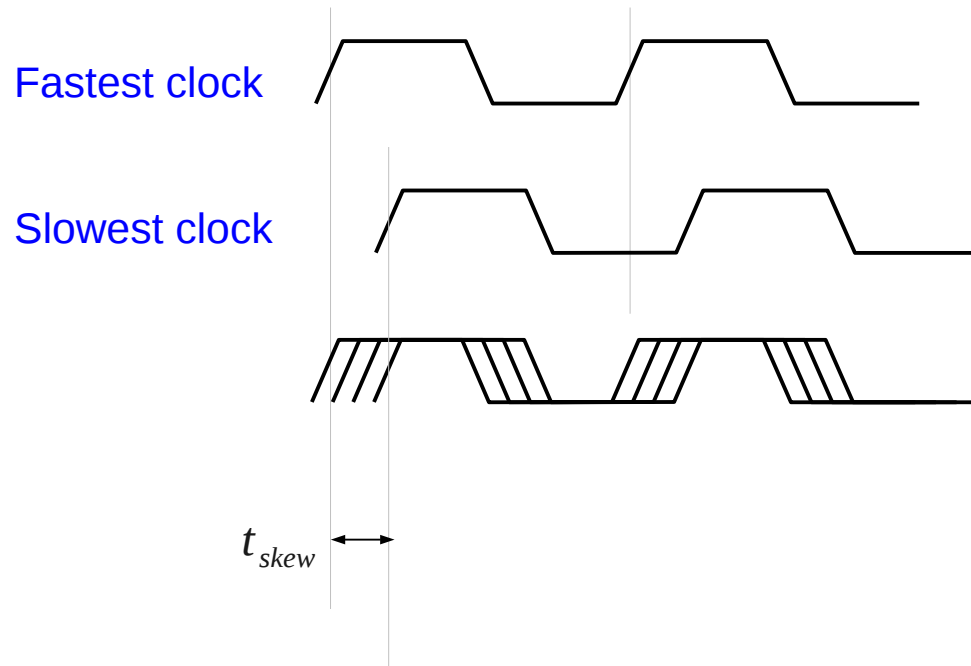
# Possible Metastable Outputs



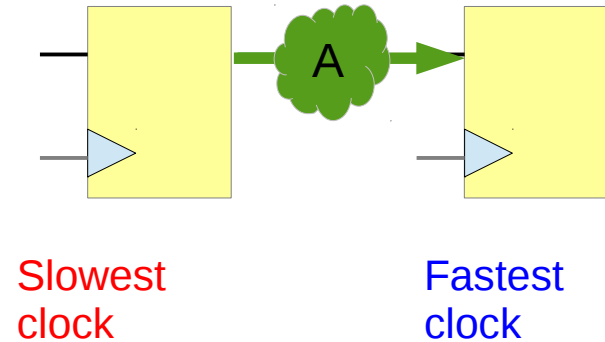
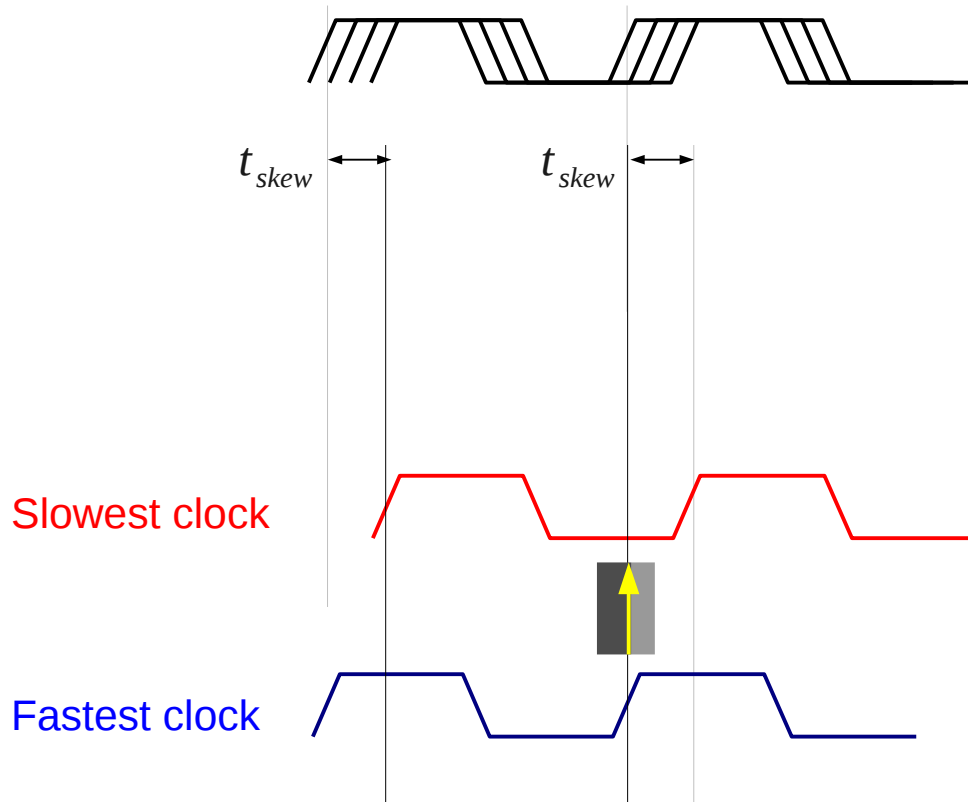
# Clock Skew



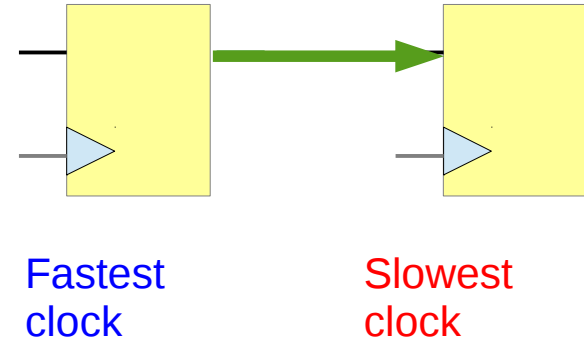
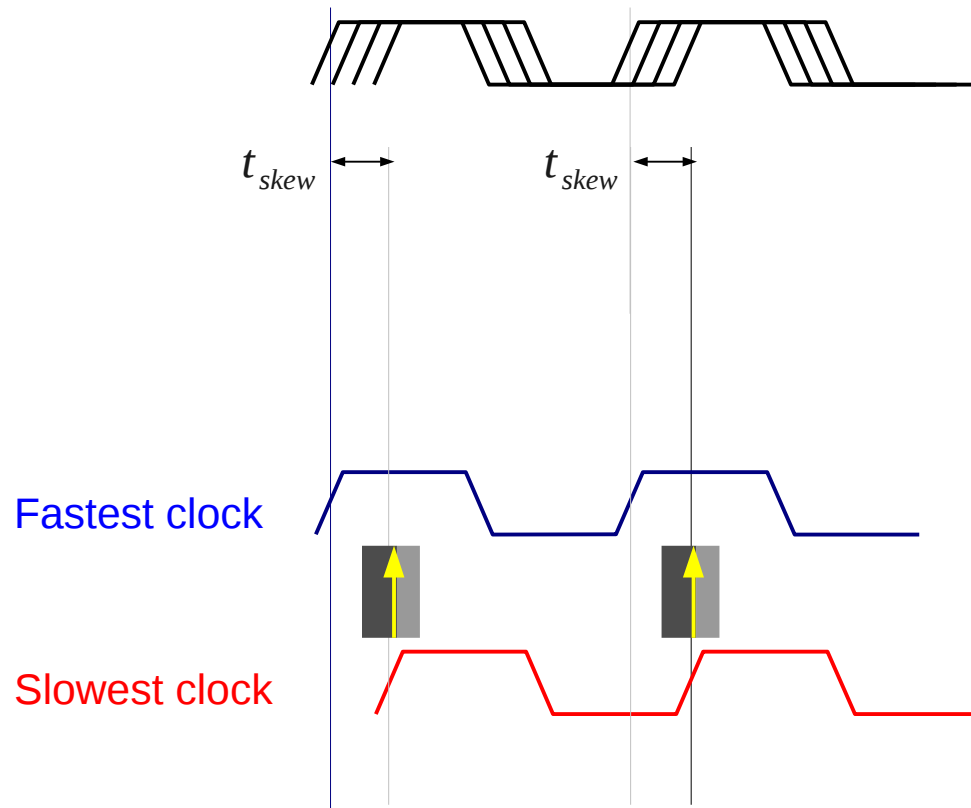
# Clock Skew



# Setup Time with Clock Skew

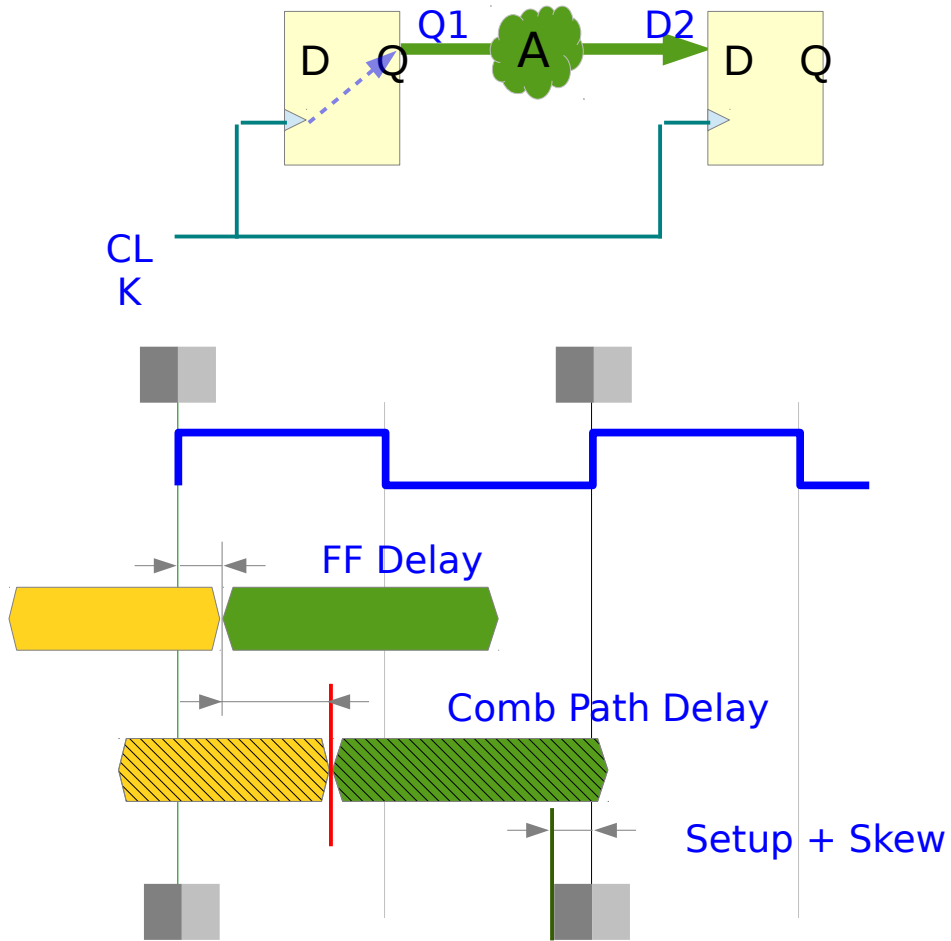


# Hold Time with Clock Skew

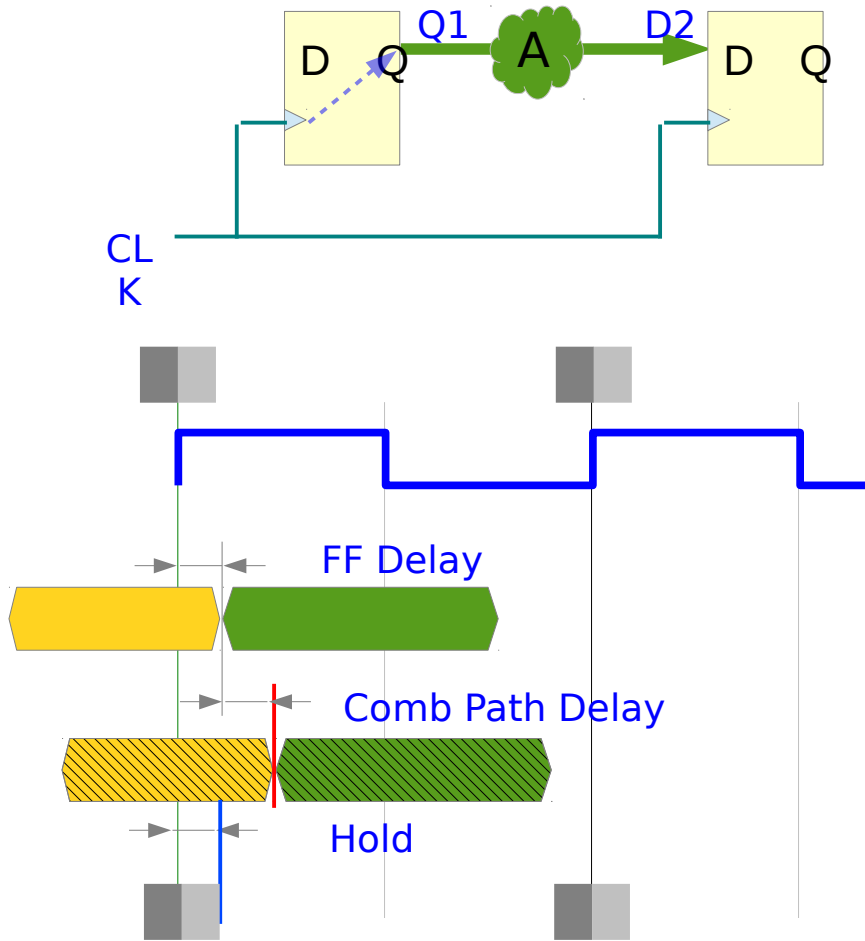




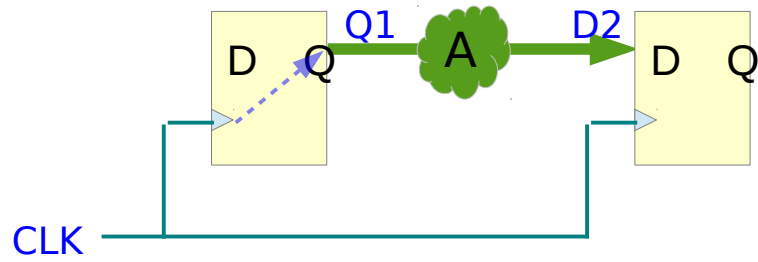
# Setup Time



# Hold Time



# Hold Time

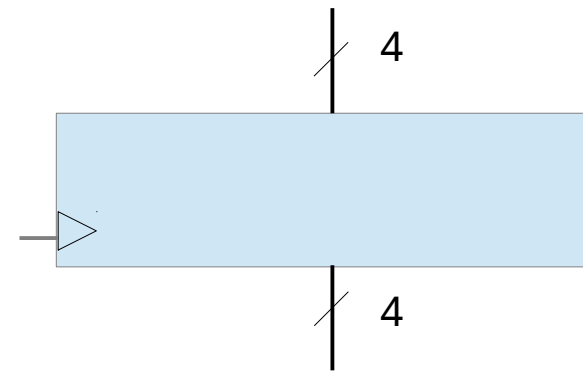
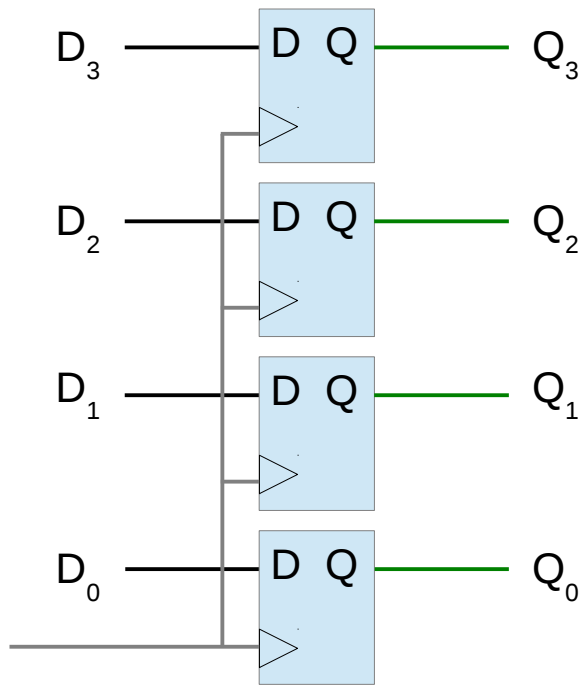
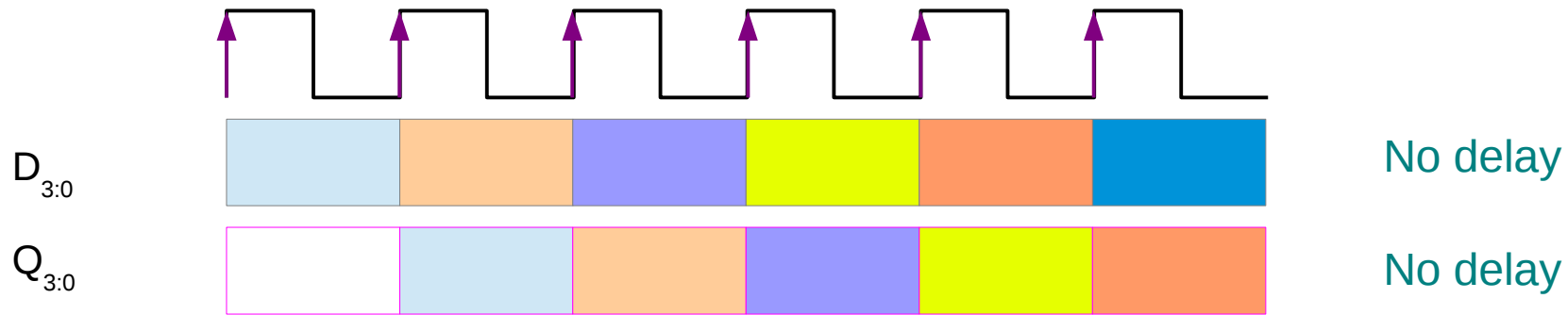


# Gate Delay

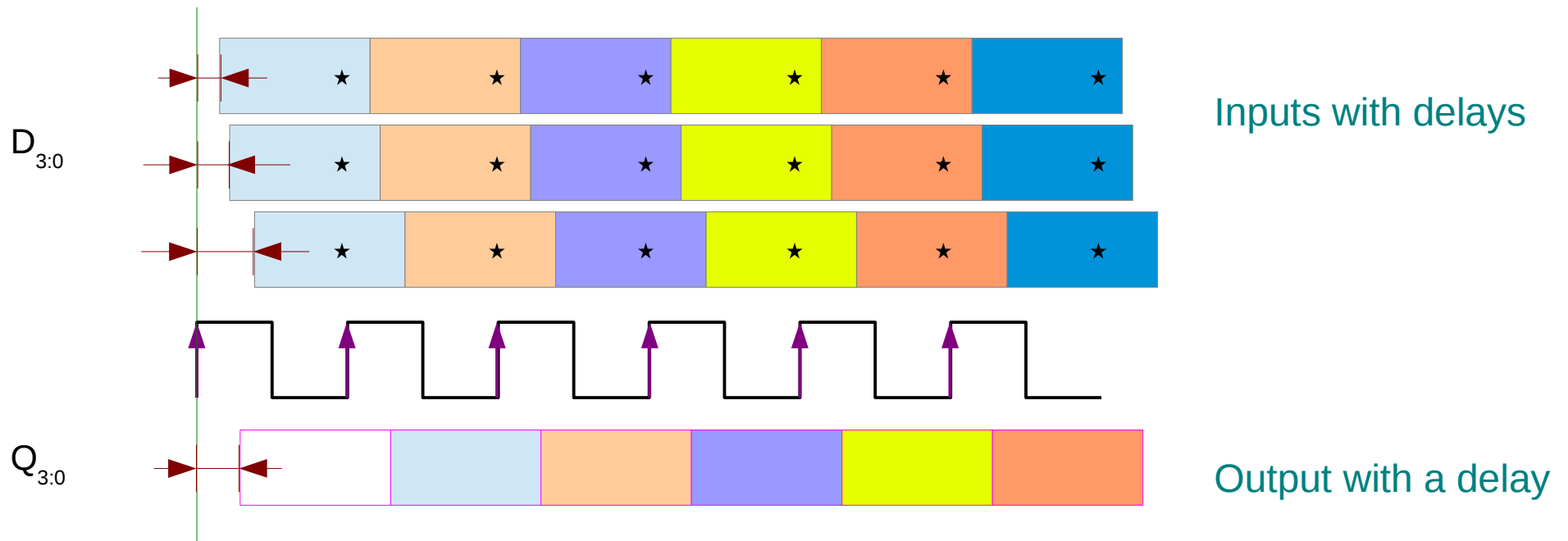
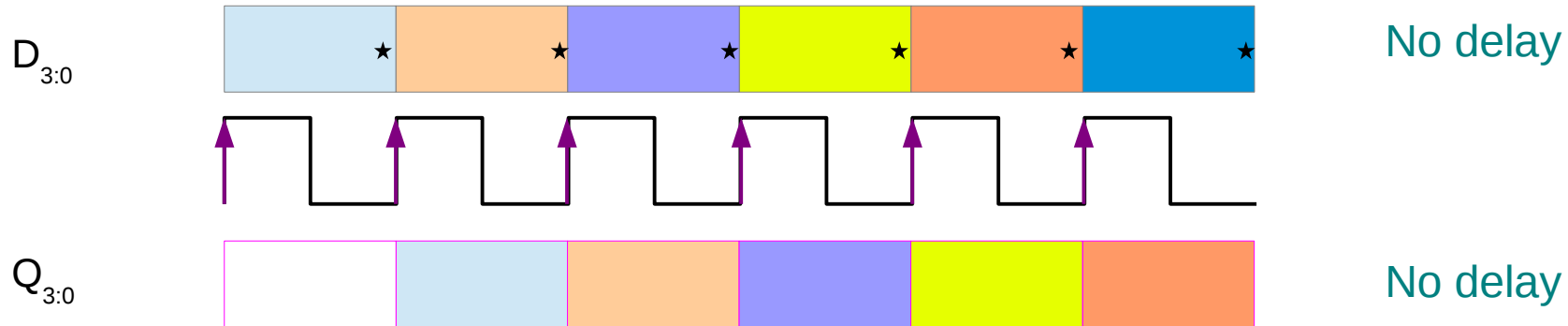
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Fan out  
Path Delay  
Max-Path  
Min-Path  
Clock  
Setup & Hold Time  
Metastability  
Synchronizer

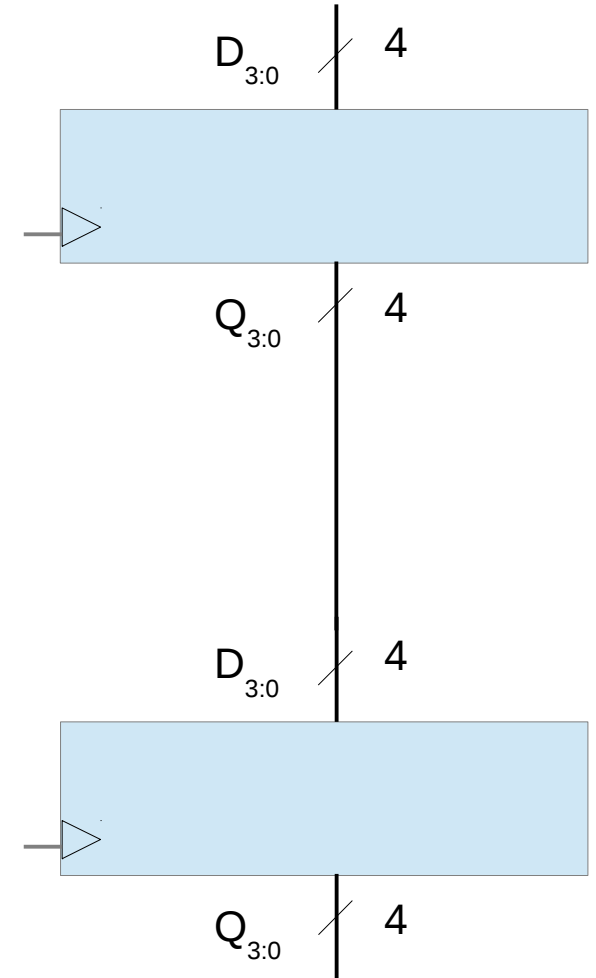
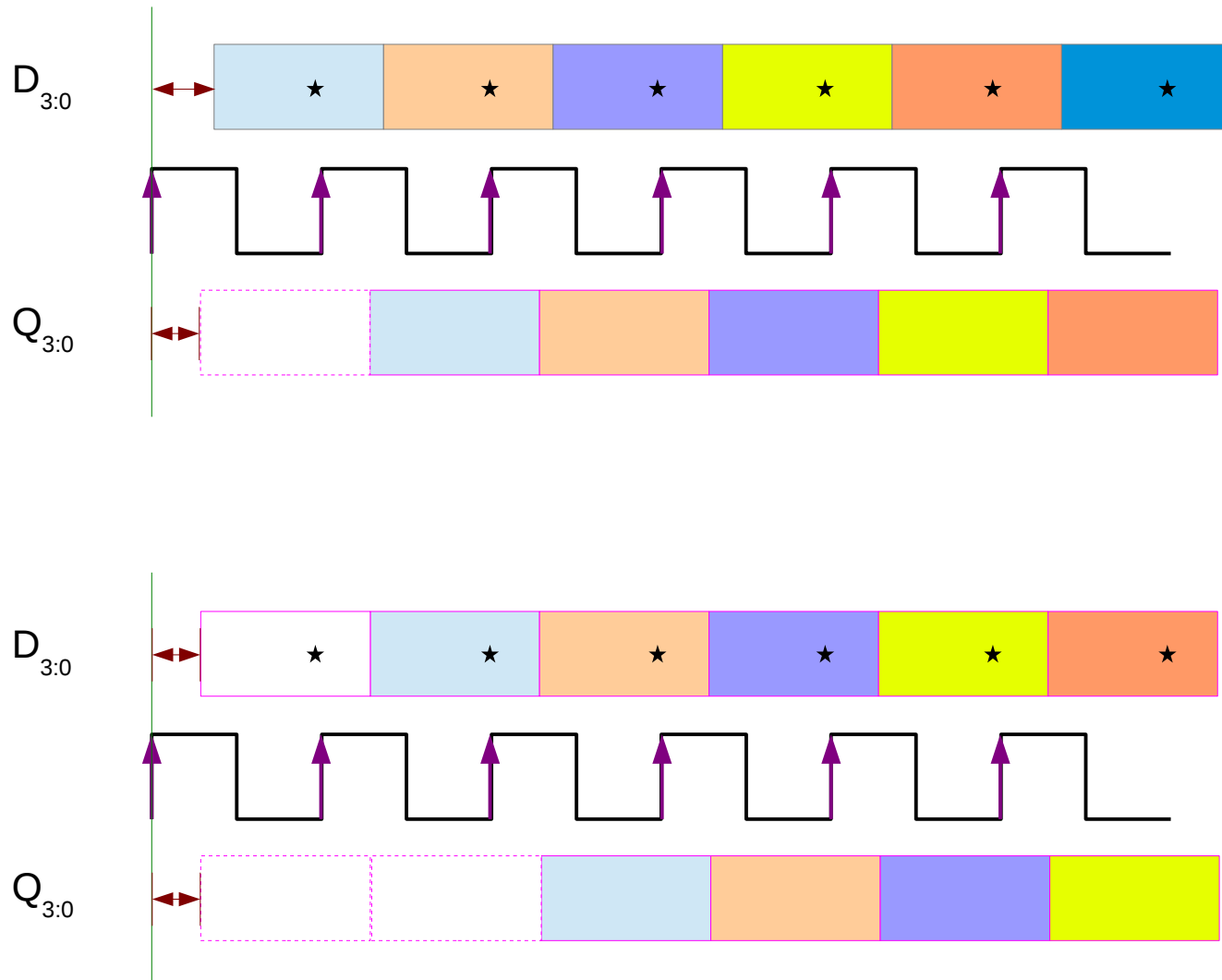
# FF Timing (Ideal)



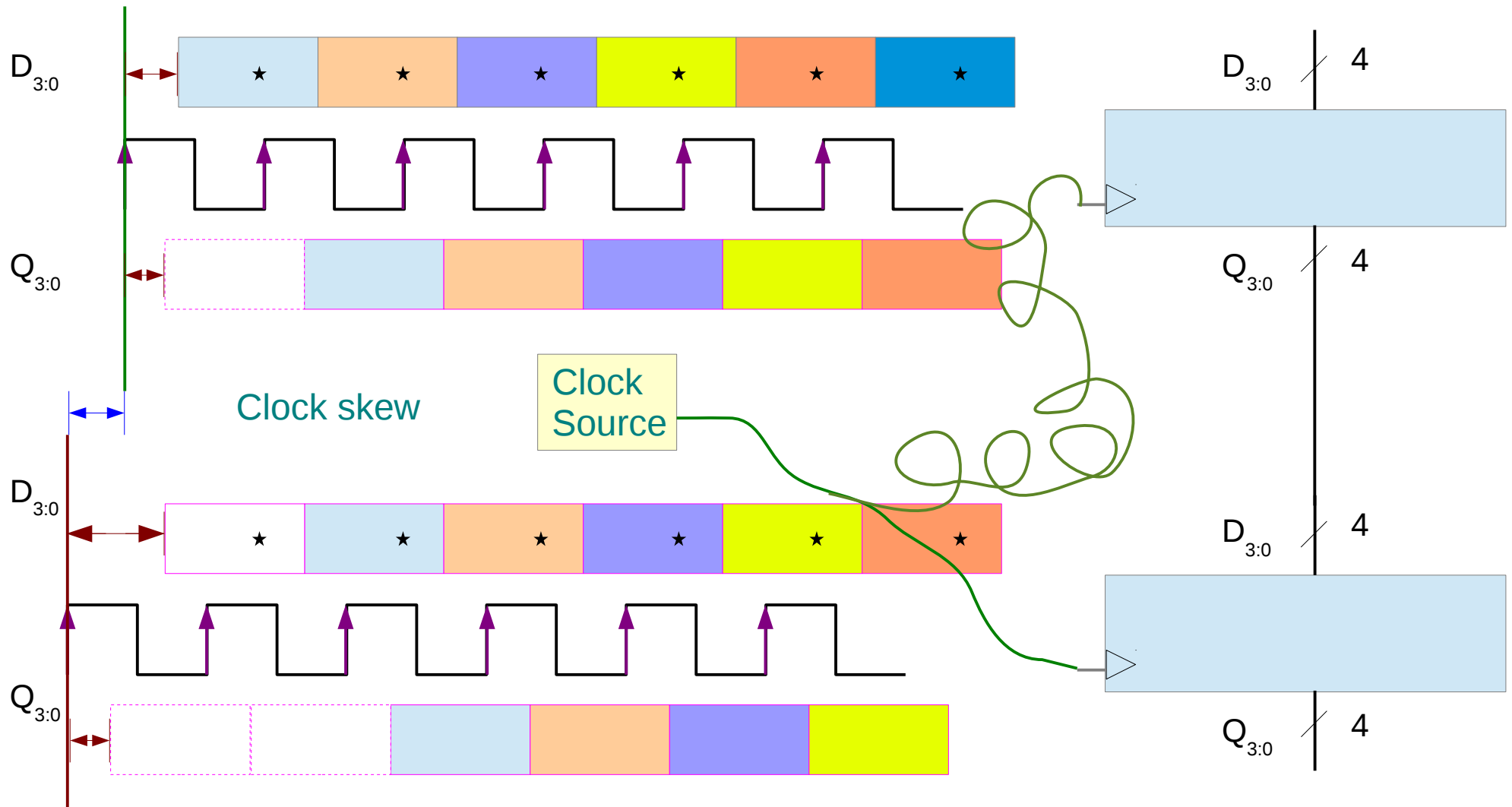
# FF Timing (Delay)



# FF Timing (Delay)

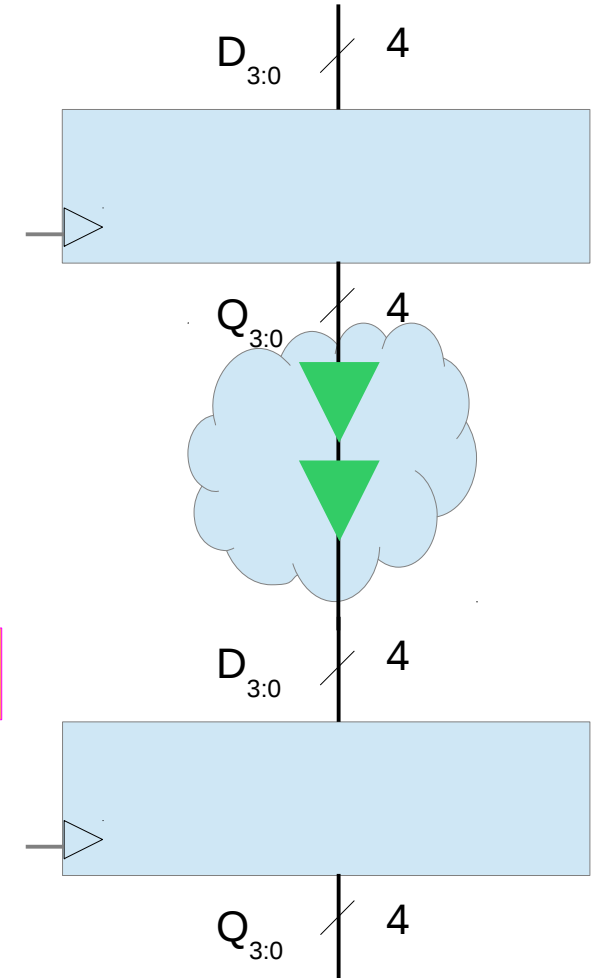
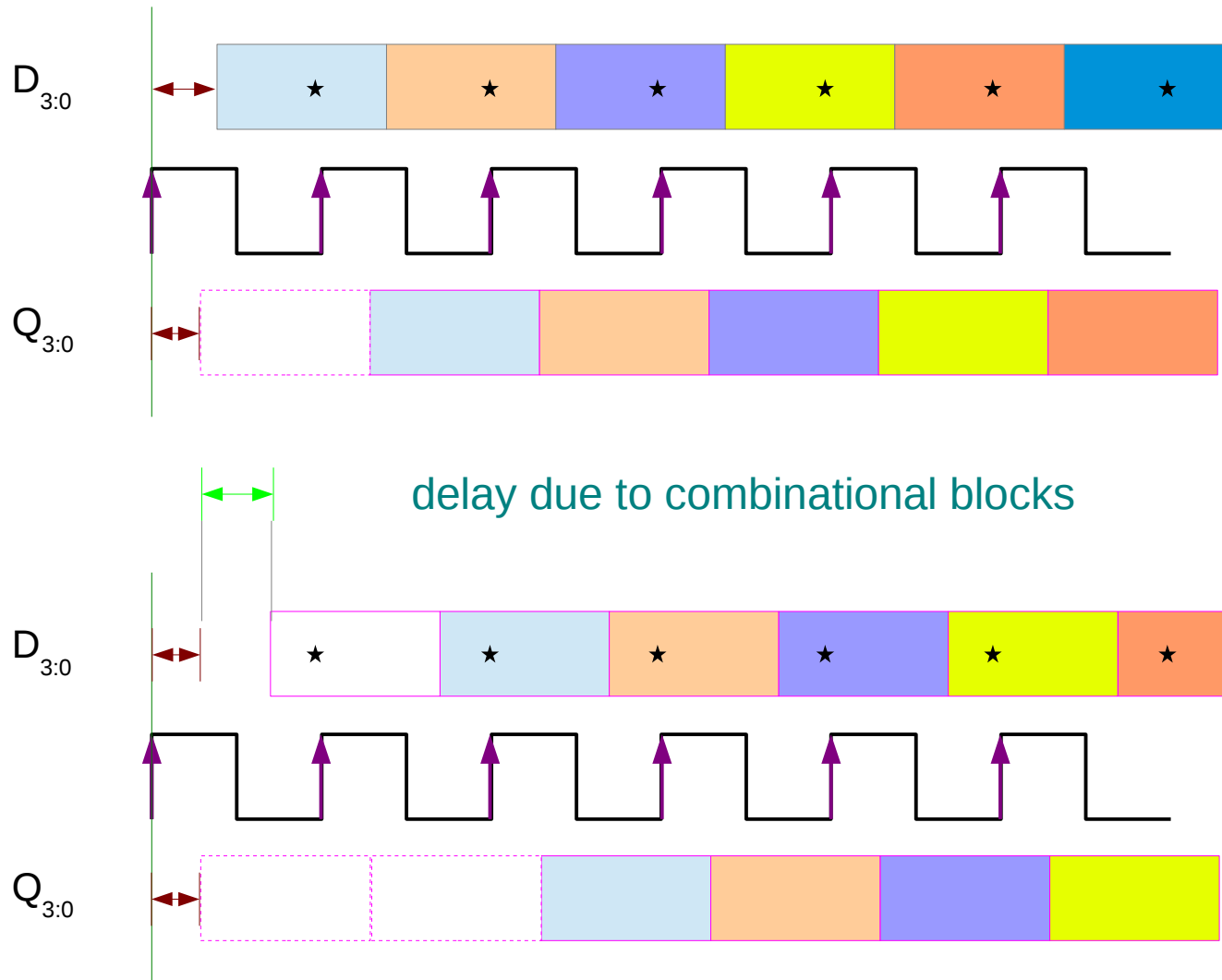


# Clock Skew

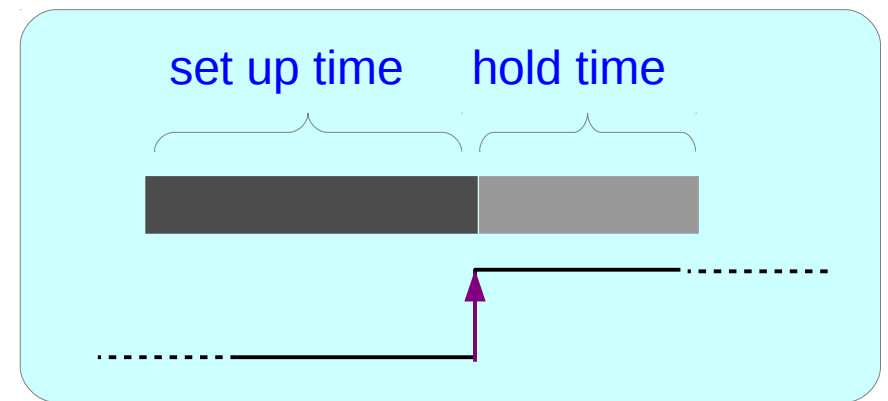
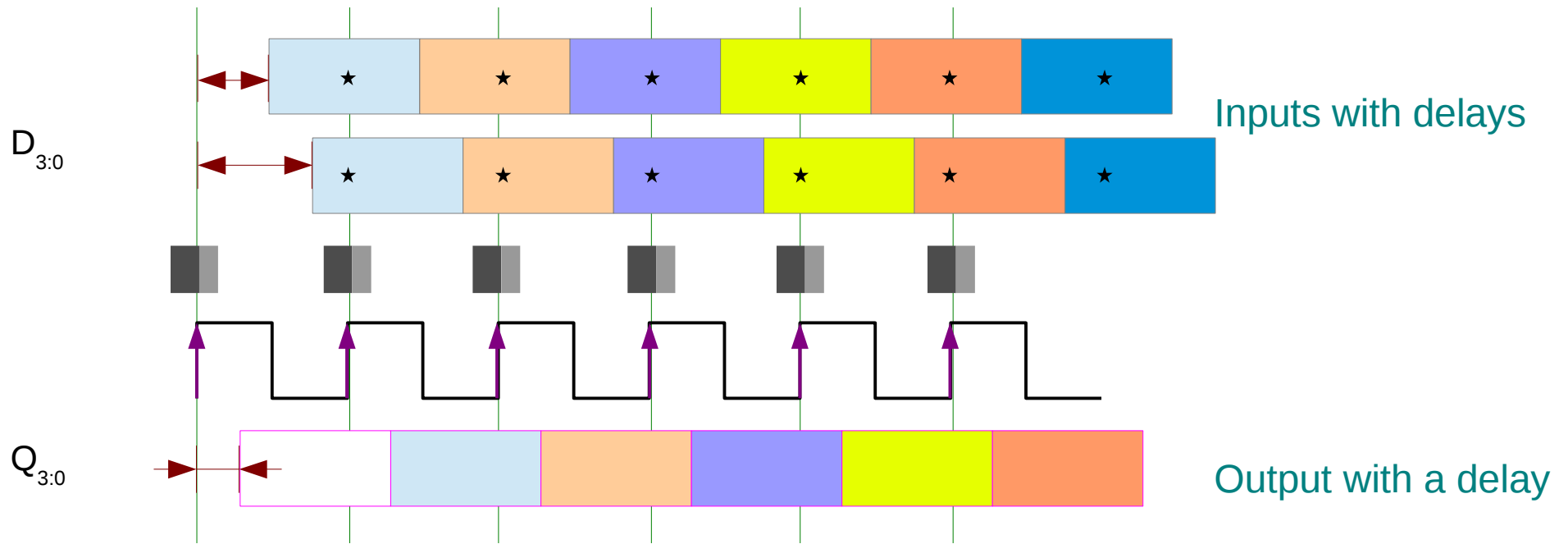




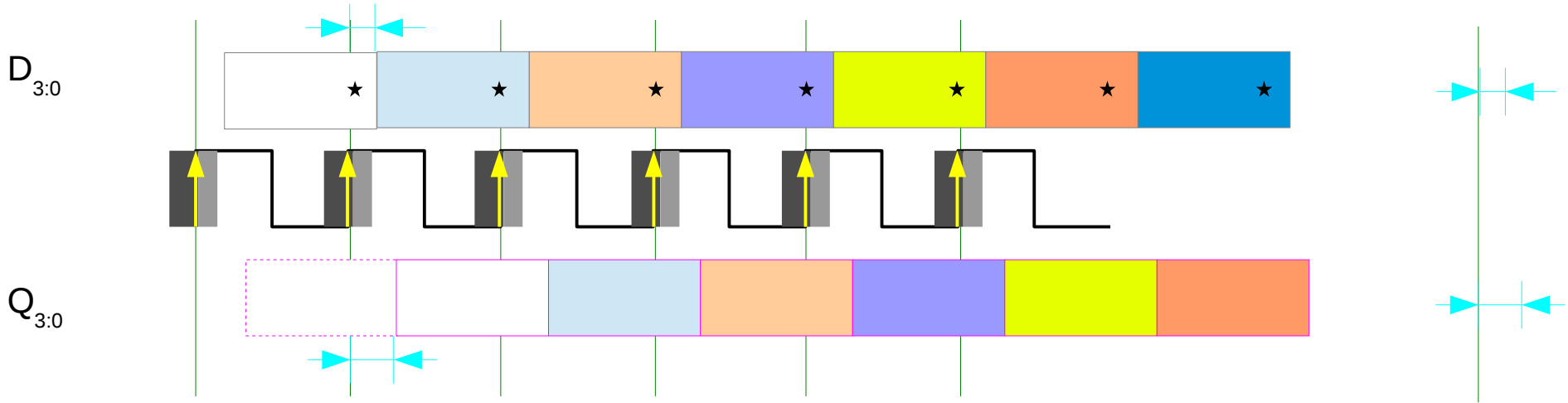
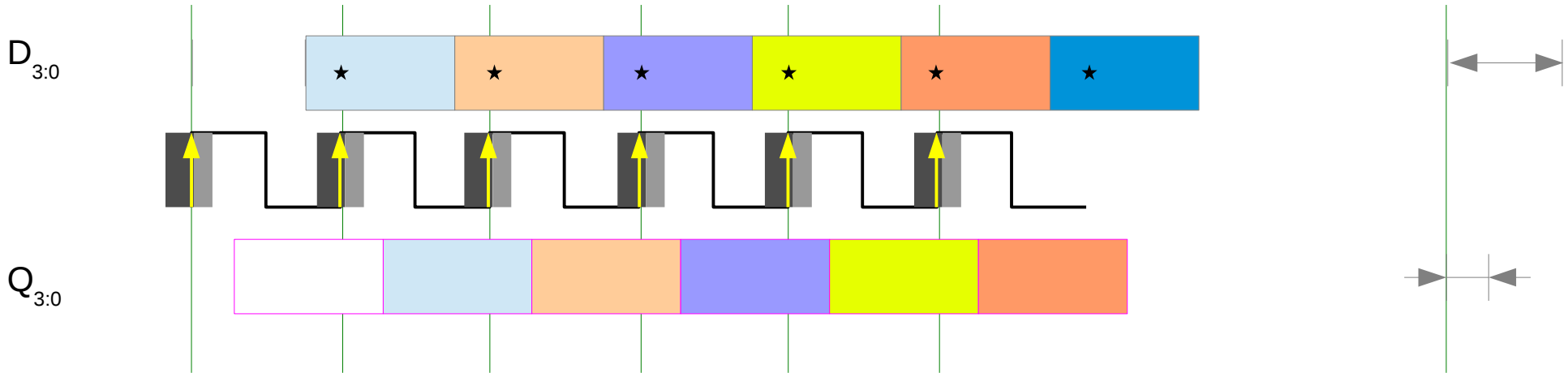
# Path Delay



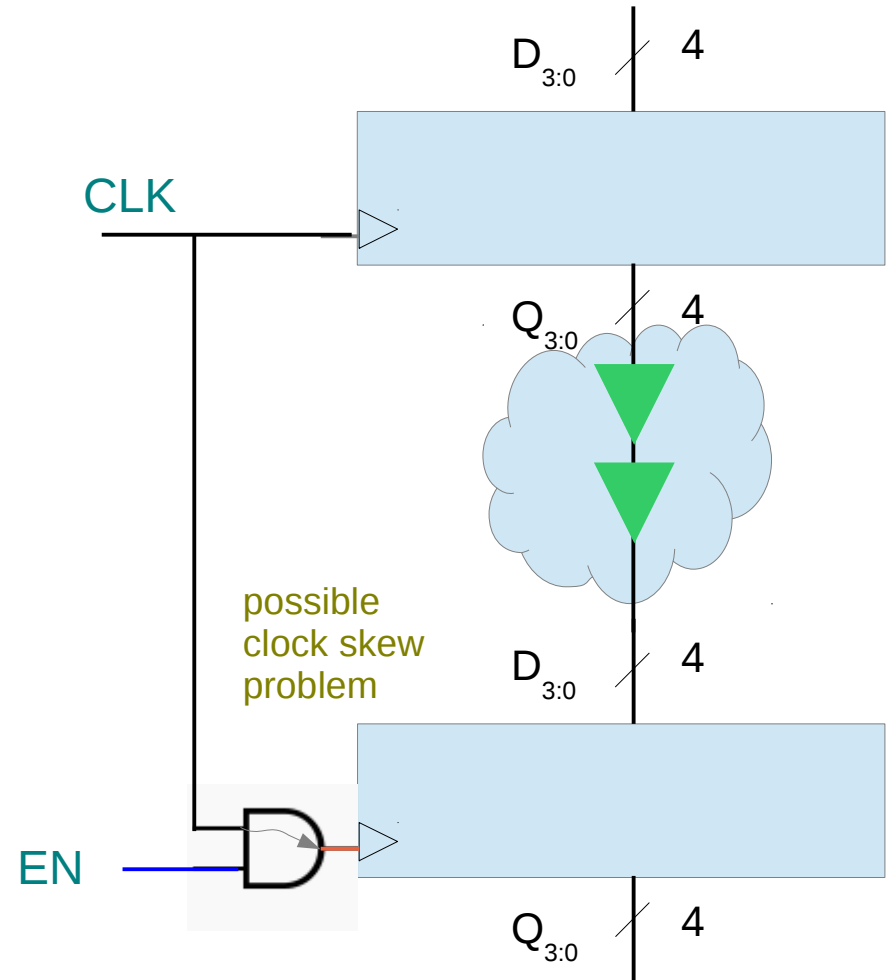
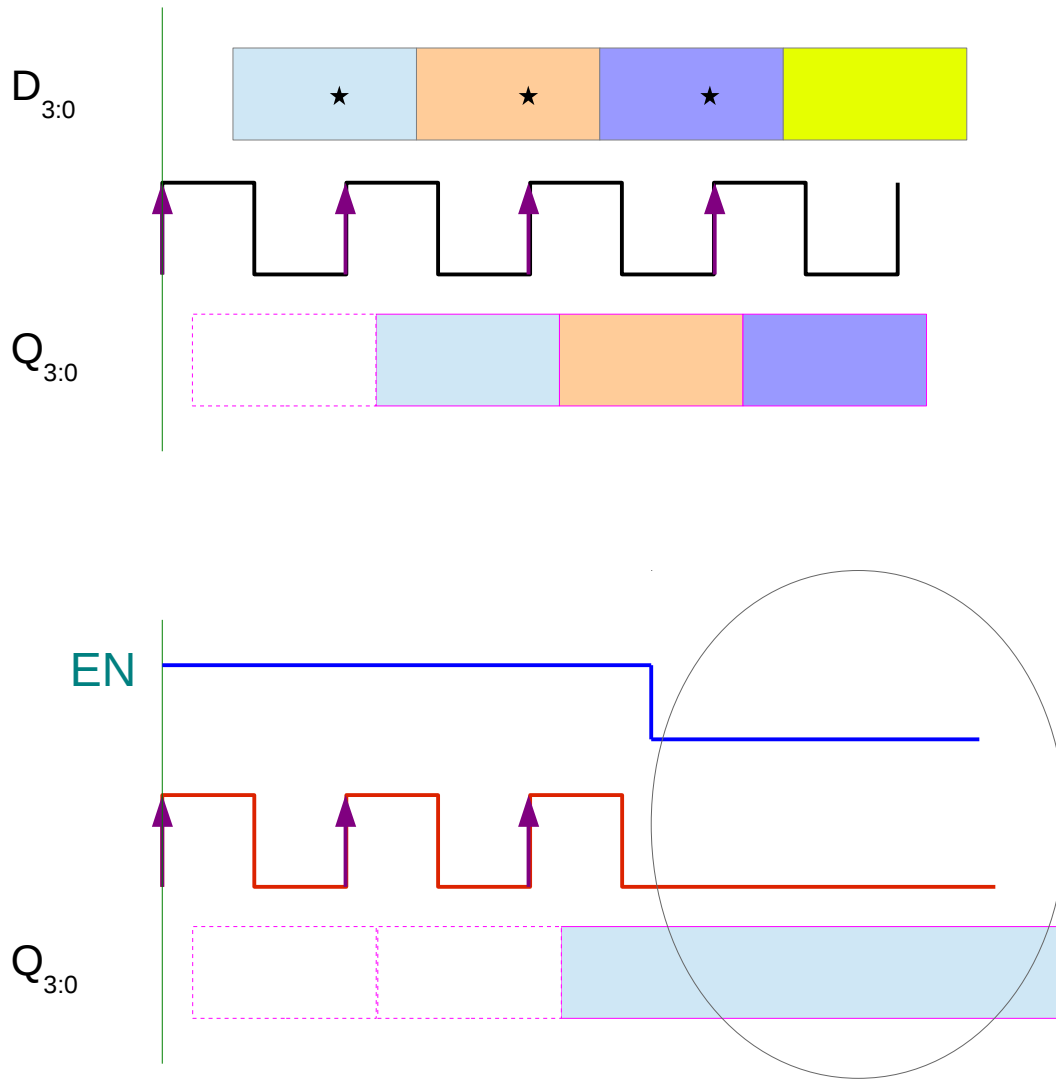
# Setup & Hold Time (1)



# Setup & Hold Time (2)



# Clock Gating



## References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_SOC\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design)
- [7] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Digital\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design)
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