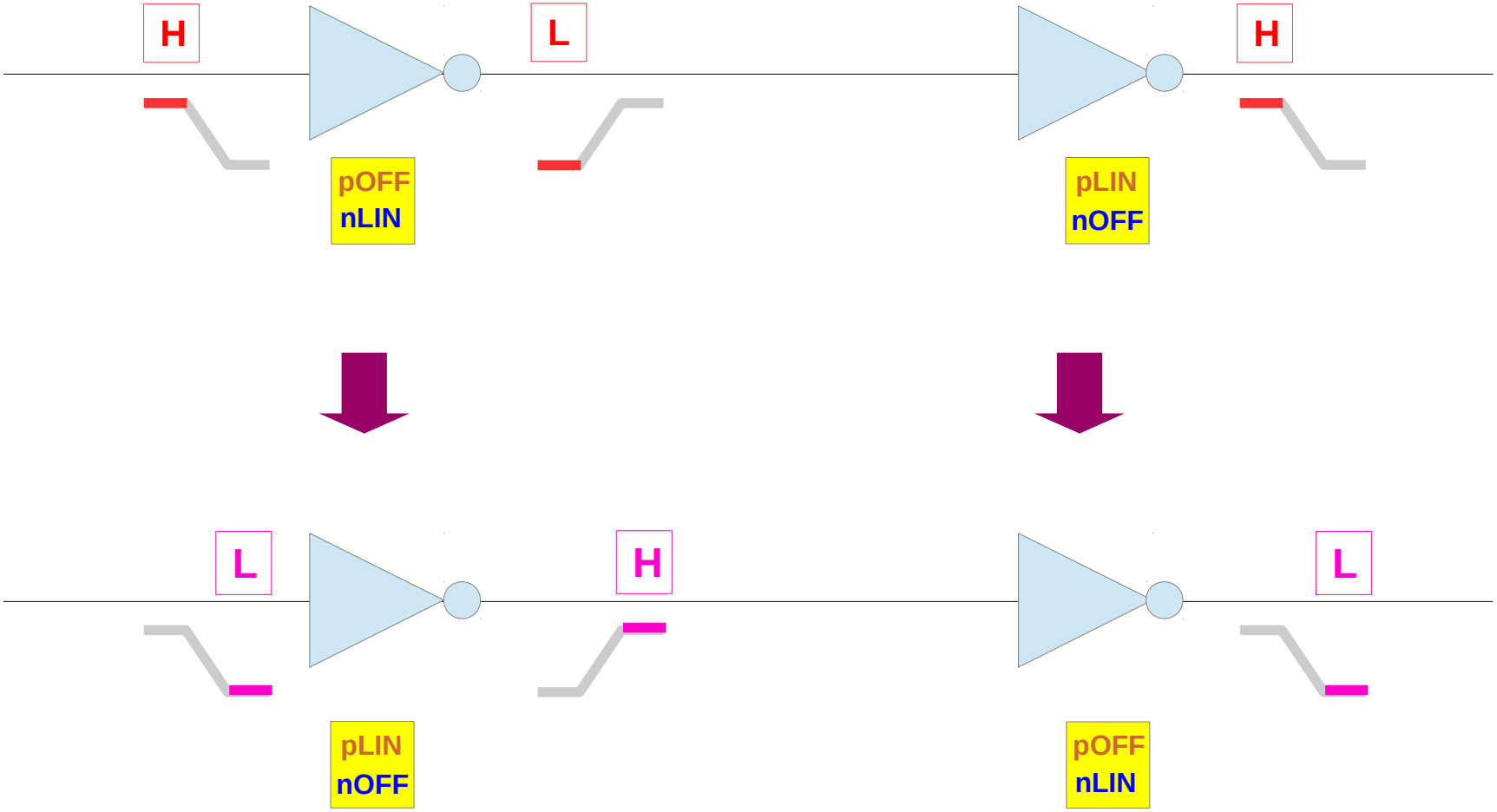
Device Delay (2F)

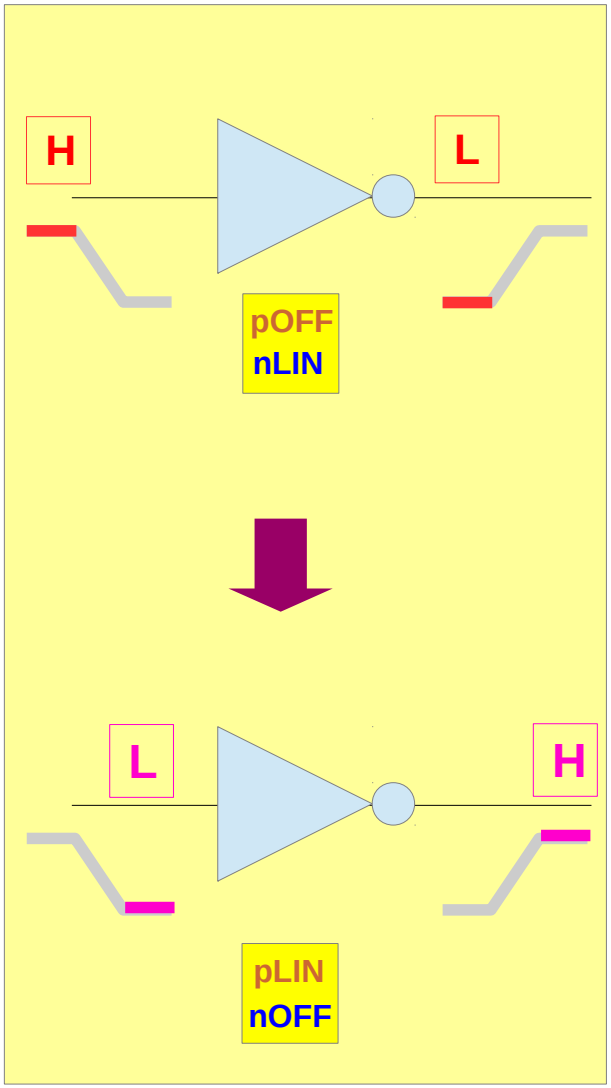
Please send corrections (or suggestions) to youngwlim@hotmail.com.

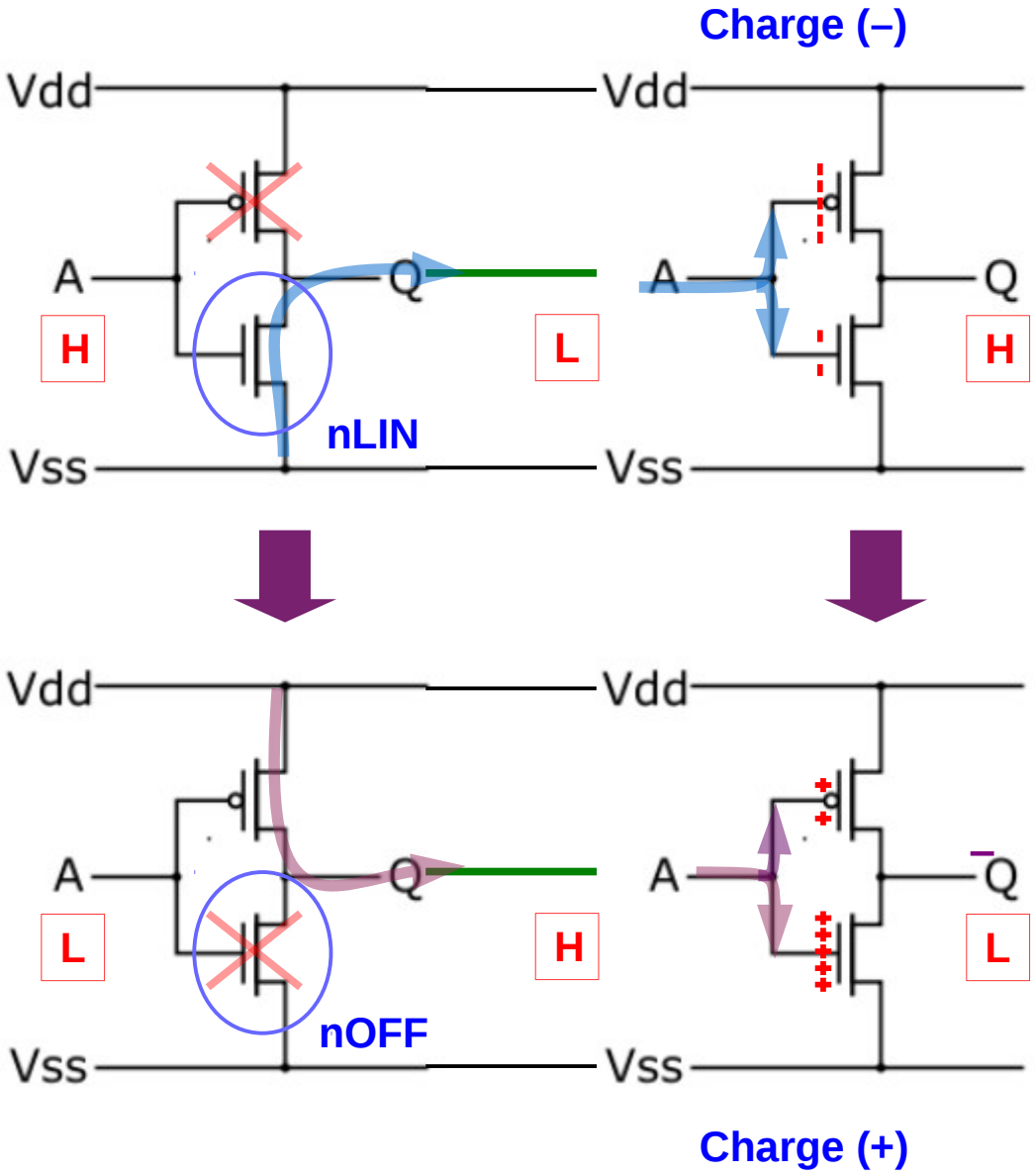
This document was produced by using OpenOffice and Octave.

Input Switching H → L

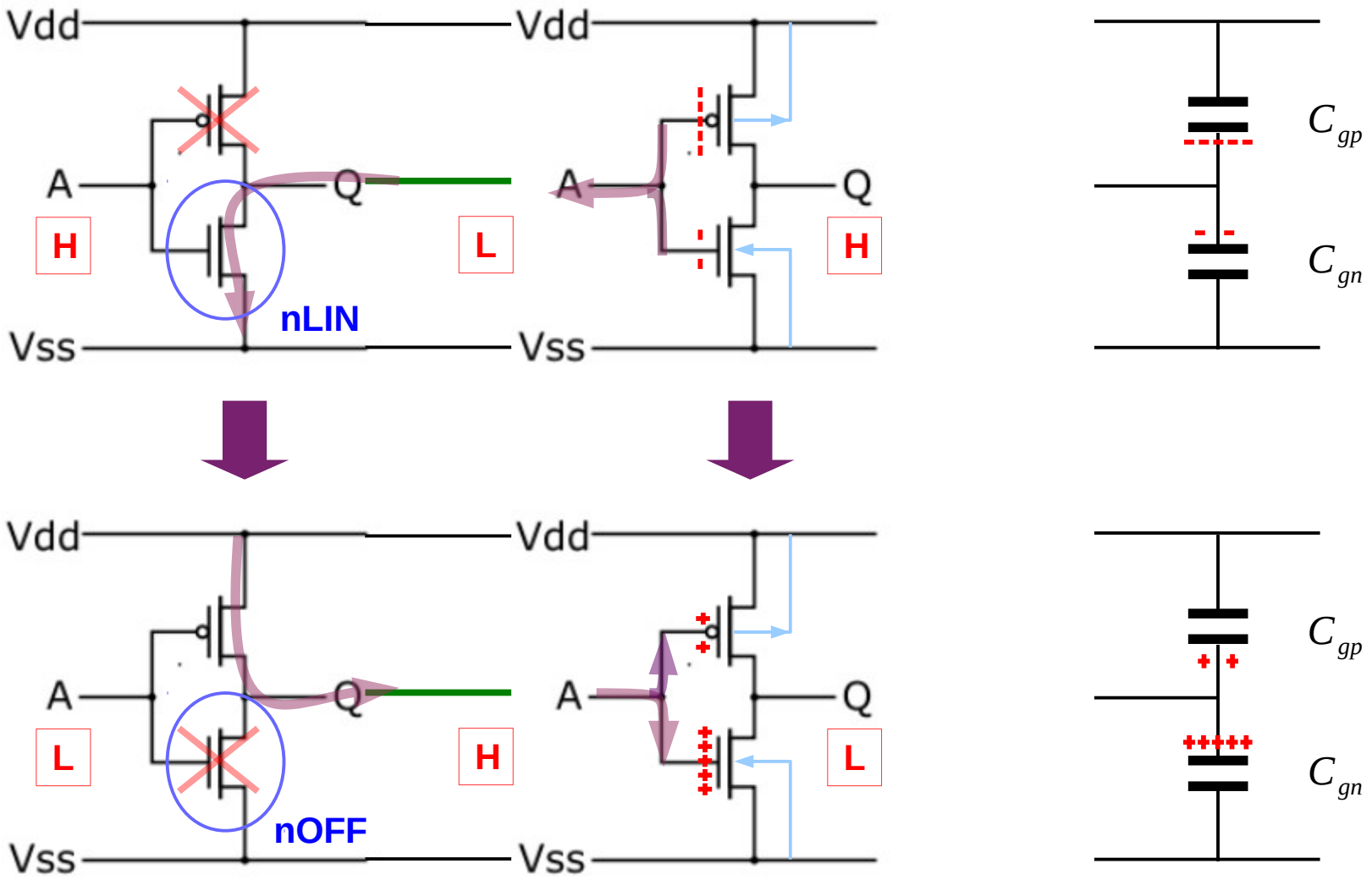


Charge (–) and (+)

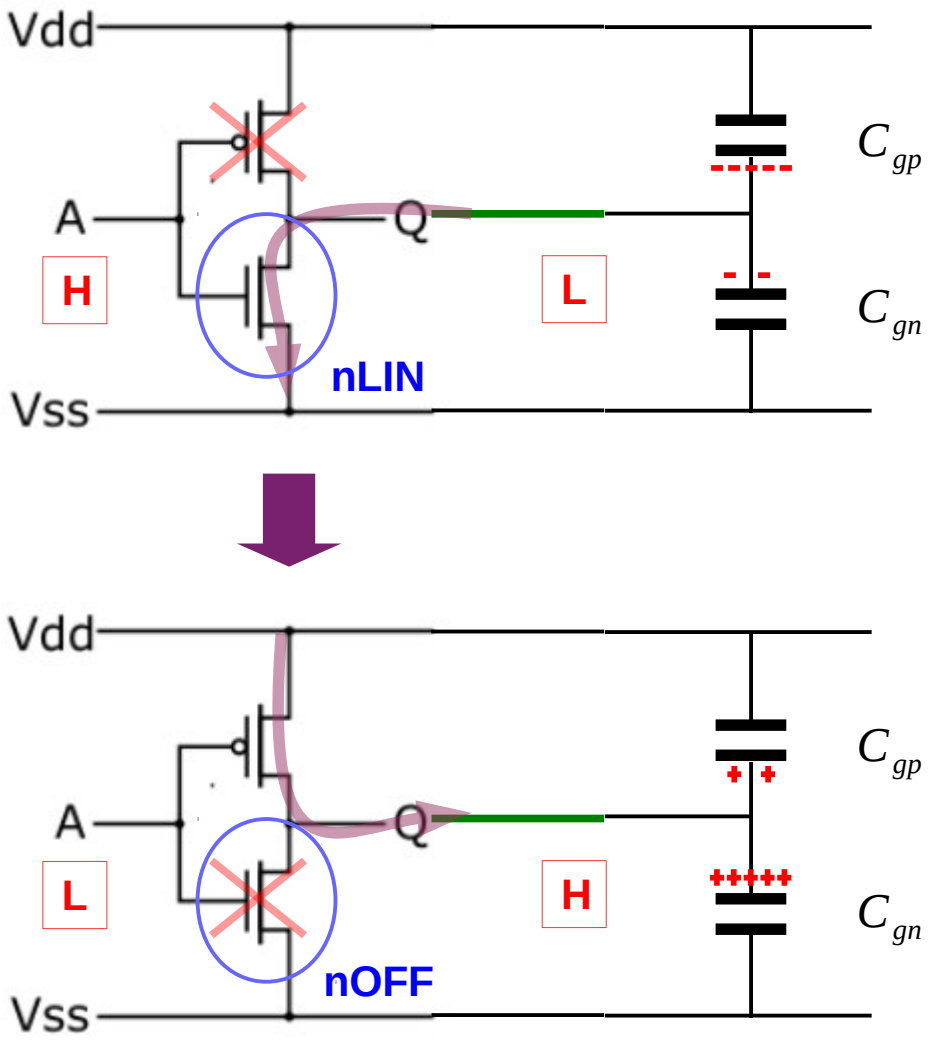

H
L
pOFF
nLIN
L
H
pLIN
nOFF


Charge (–)
Vdd
Vdd
A
Q
H
L
nLIN
Vss
Vss
A
Q
H
Vdd
Vdd
A
Q
L
H
nOFF
Vss
Vss
A
Q
L
Charge (+)

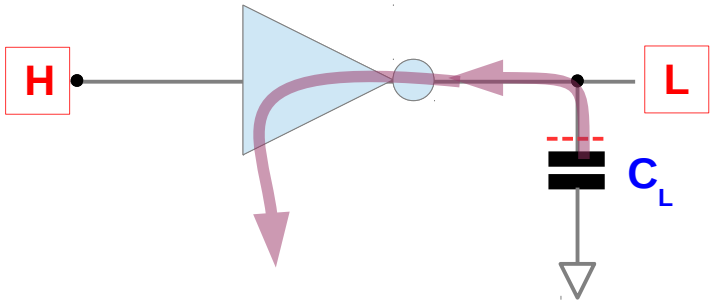
Gate Capacitances



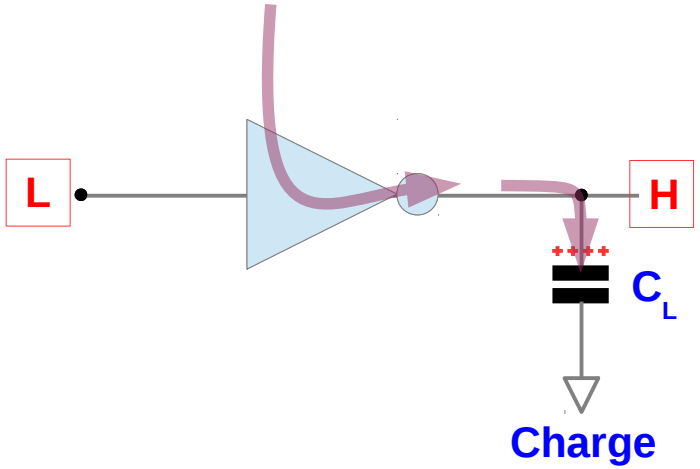
Load Capacitance Model



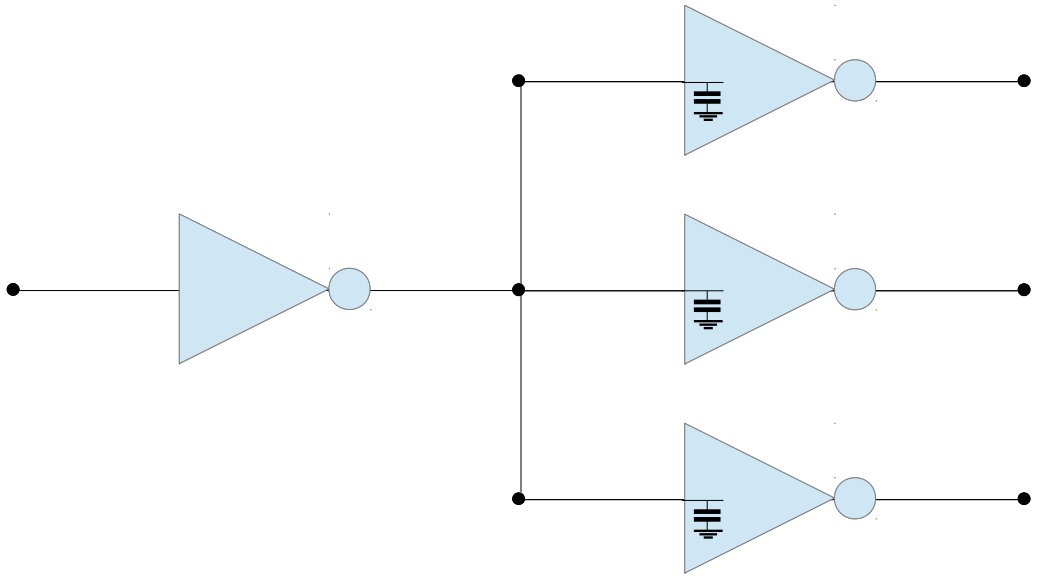
Charge (–) ⬌ **Discharge (+)**



$$C_L = C_{pn} + C_{gn}$$



Load Capacitance



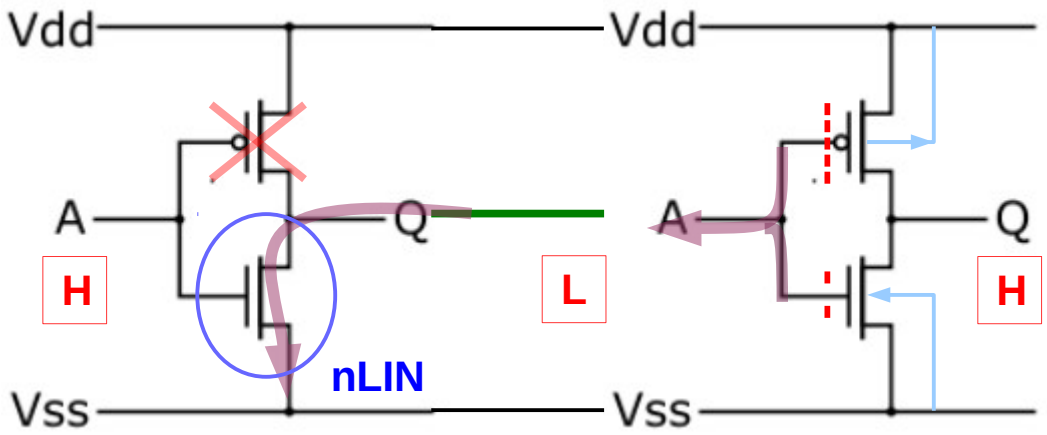
$$C_L = 3C_g$$

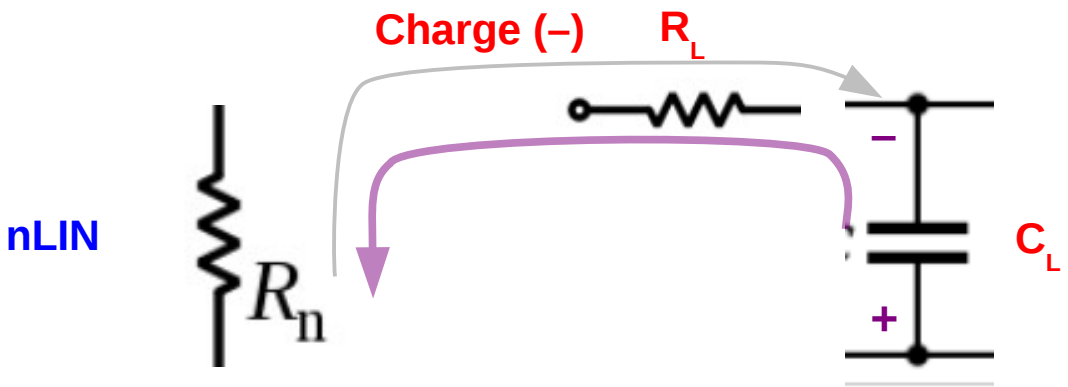
Big Capacitance

- A signal connected off-chip
- A signal with very long wire
- A clock signal driving many flip-flops

Fall Time

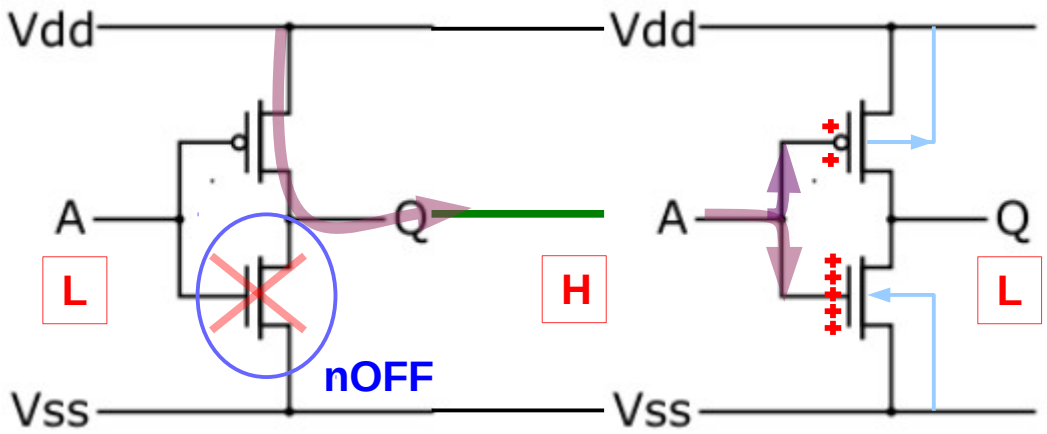
https://en.wikipedia.org/wiki/

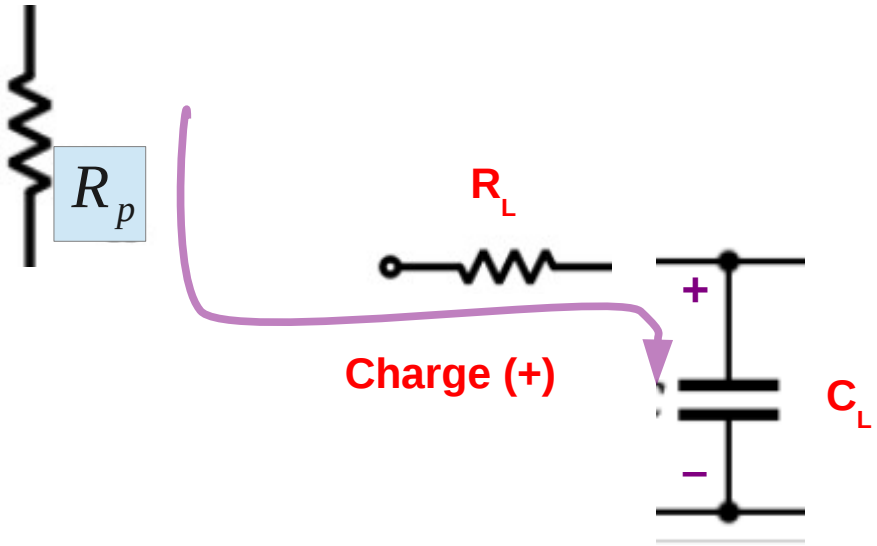




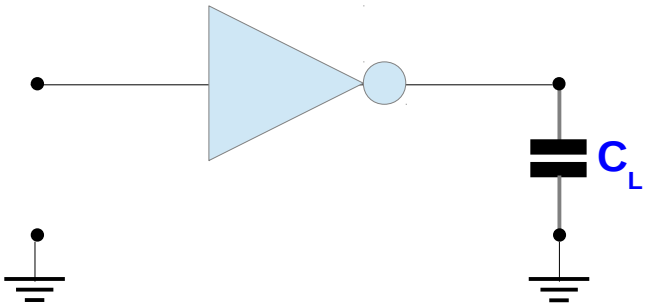
Rise Time

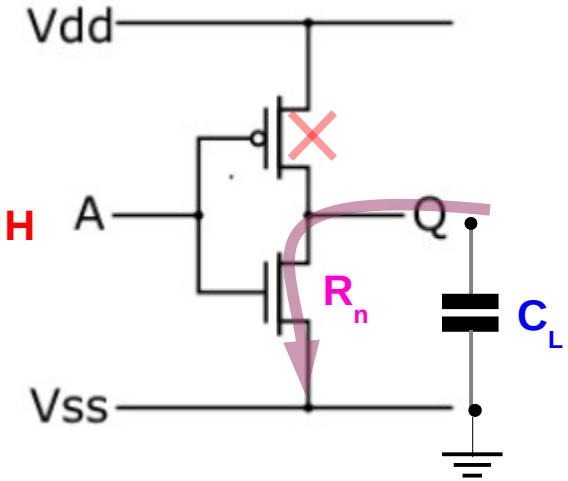
https://en.wikipedia.org/wiki/

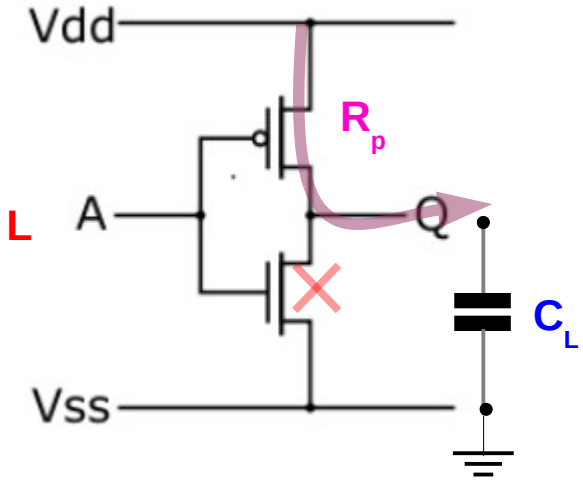




Rising and Falling Time

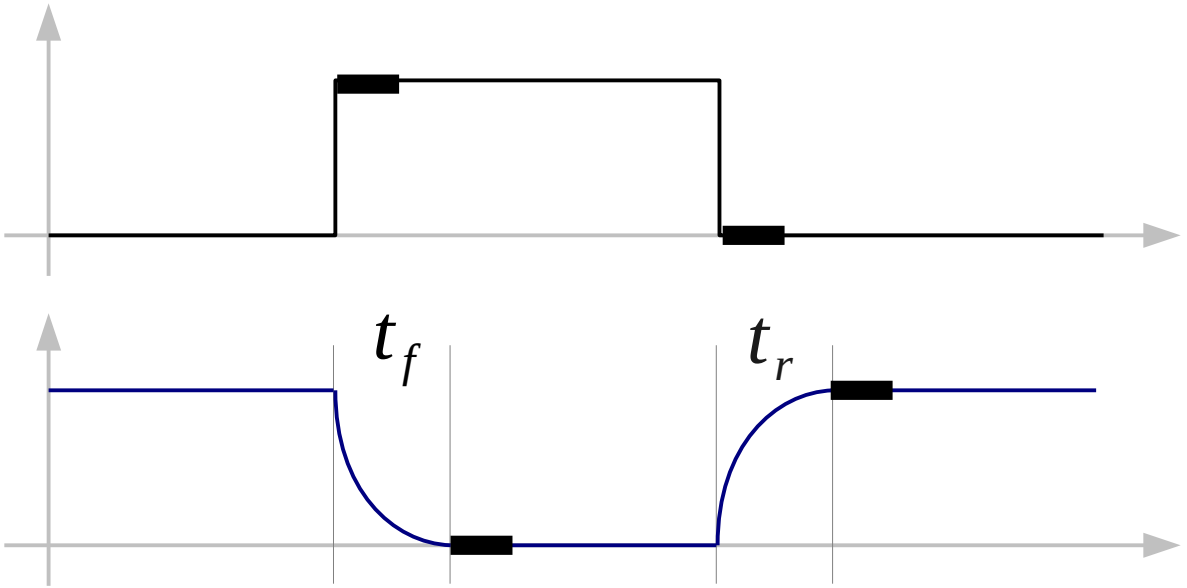






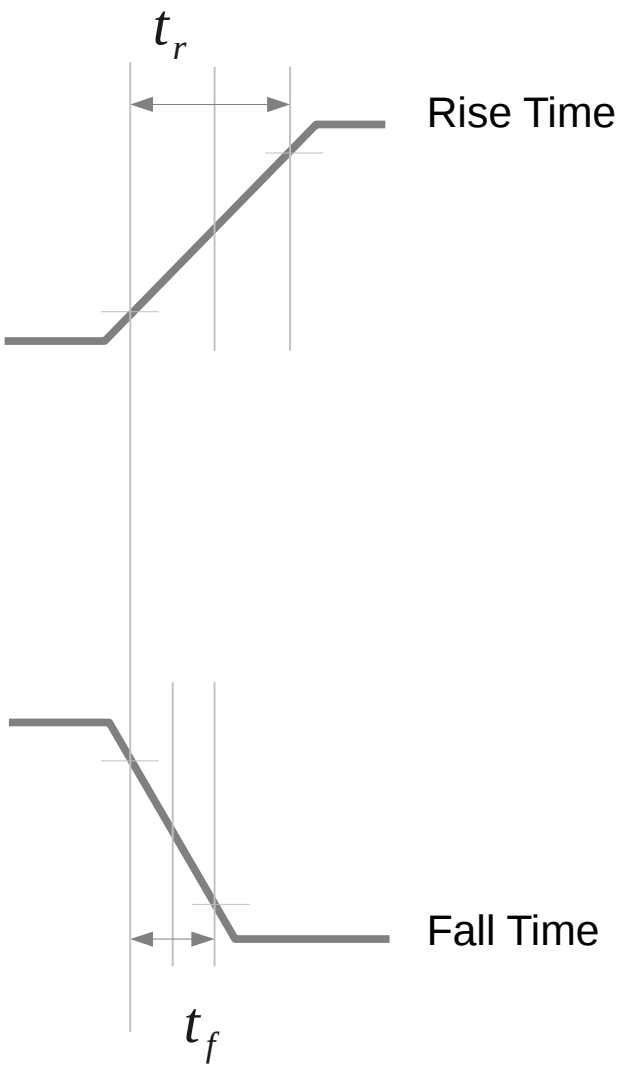
$$t_f \propto R_n C_L$$

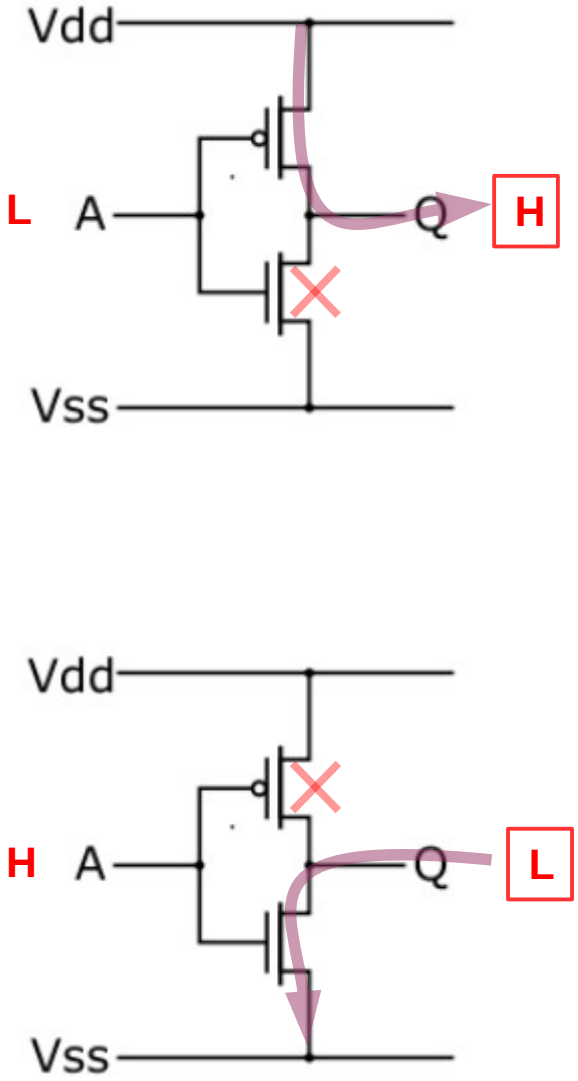
$$t_r \propto R_p C_L$$



Rising and Falling Time (1)

$R_n < R_p$



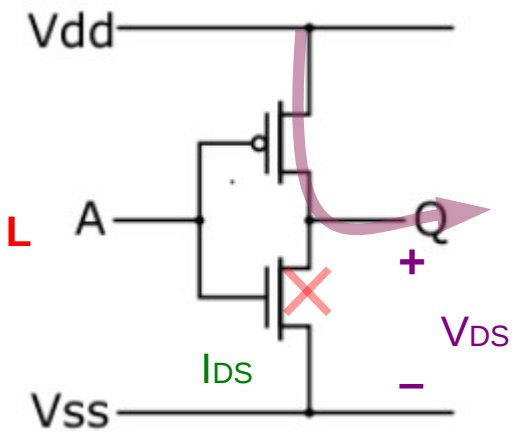


$$\frac{\beta_n}{\beta_p} > 1 \qquad \frac{R_n}{R_p} < 1$$

$$\frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$

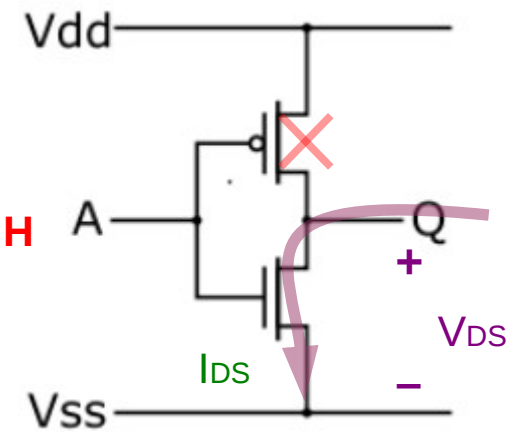
$$\frac{t_f}{t_r} = \frac{2.2\,\tau_n}{2.2\,\tau_p} < 1$$

Rising and Falling Time (2)



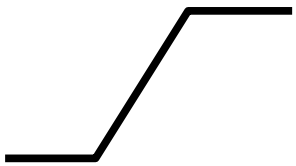
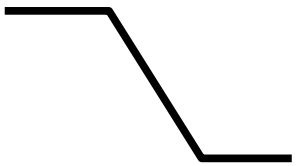
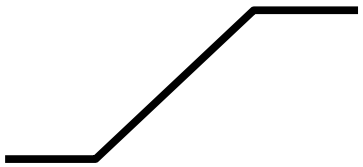
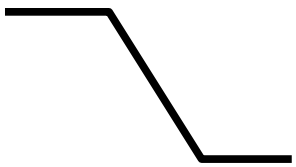
Rise Time

$$t_r = R_p C_L$$

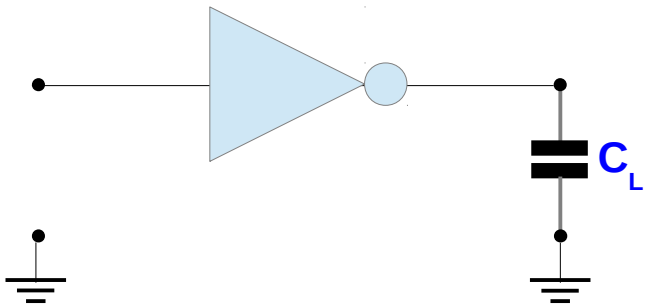


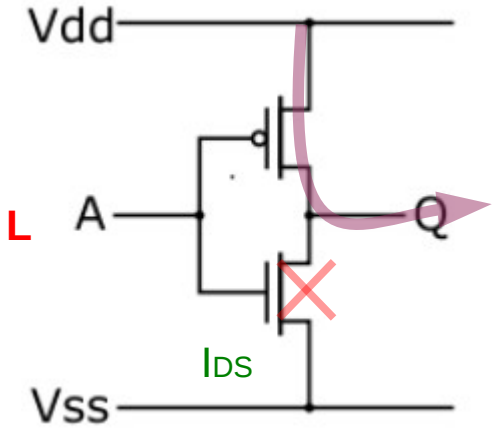
Fall Time

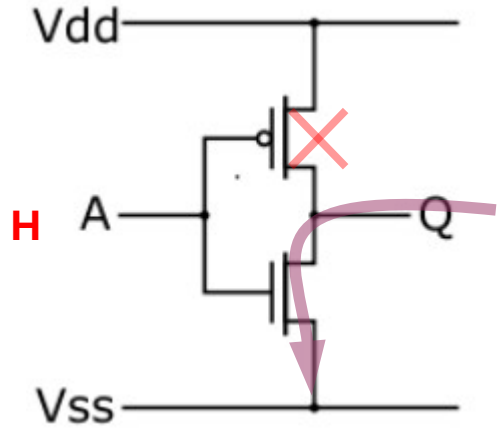
$$t_f = R_n C_L$$

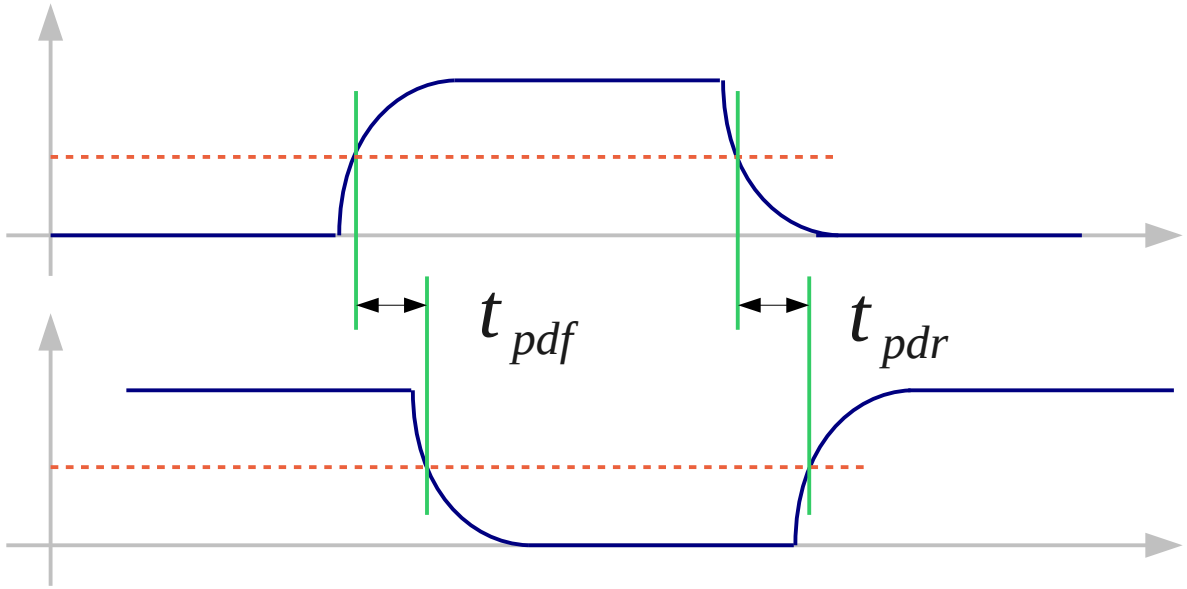
$\frac{\beta_n}{\beta_p} = 1.0$ $R_n = R_p$		
$\frac{\beta_n}{\beta_p} = 2.0$ $R_n < R_p$		

Propagation Delay









Characteristic Curve

References

[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”